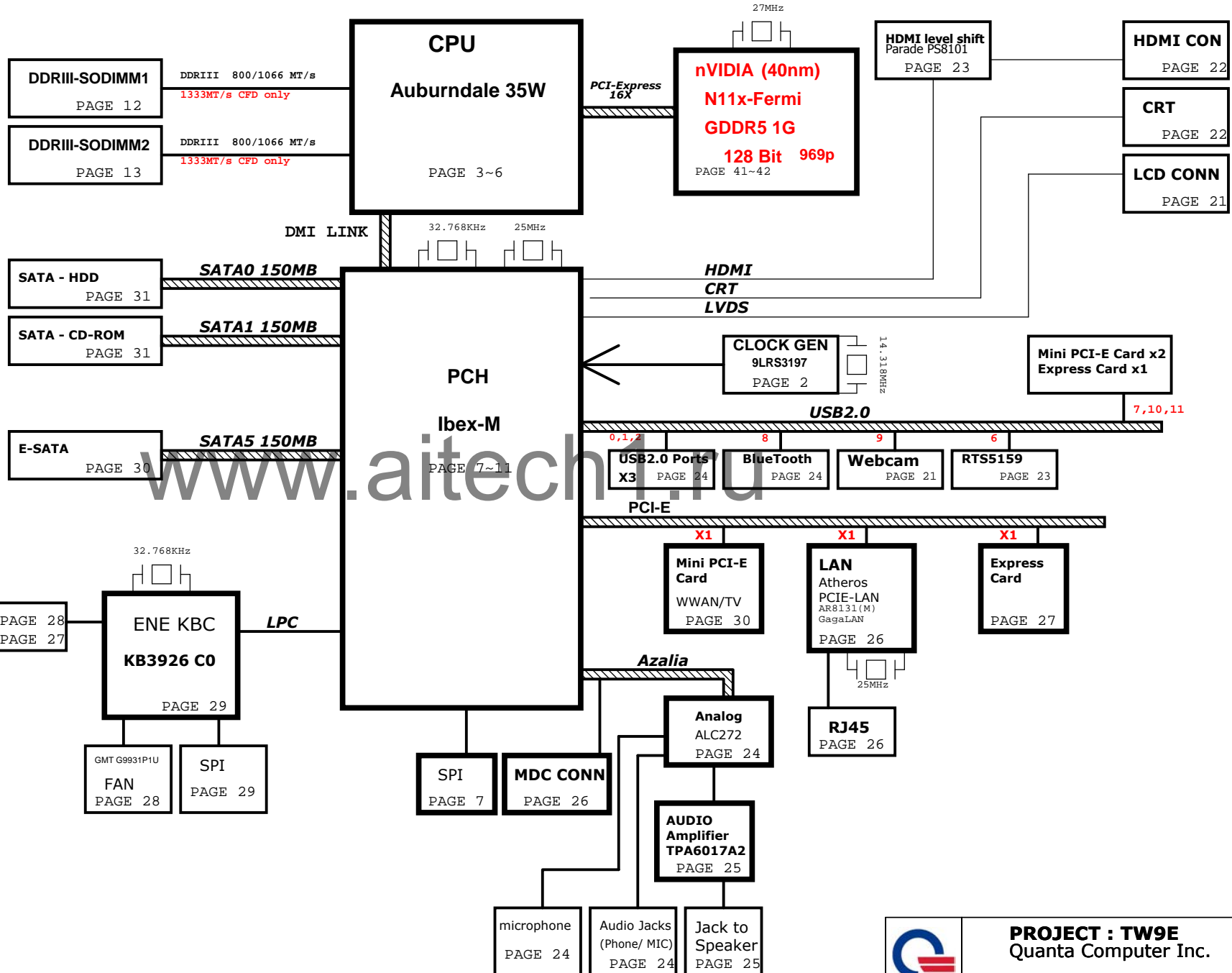


TW9E (15.6W) BLOCK DIAGRAM

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT



UMA GPU CORE (RT8152A)	PAGE 32
SYSTEM POWER RT8206B	PAGE 33
VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204)	PAGE 34
CPU CORE ISL6288	PAGE 35
VGACORE(1.025V) RT8208A	PAGE 36
DDR III SMD DR_VTERM 1.5V/1.5VSUS(RT8207)	PAGE 37
SYSTEM CHARGER(ISL6251AHAZ-T)	PAGE 39

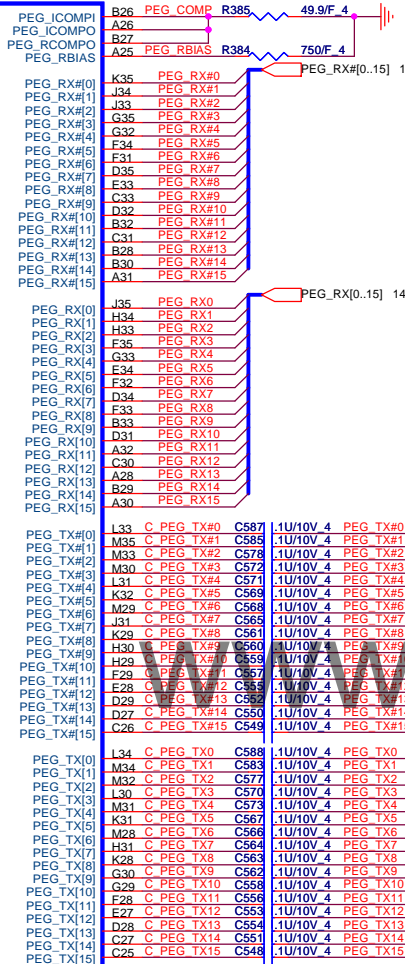
	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

U29A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS



IC:AUB_CFD_TPGA,R1P0

2.7GT/s data rate

9 FDI_TXN[7:0]

9 FDI_TXP[7:0]

9 FDI_TXN[7:0]

9 FDI_TXP[7:0]

9 FDI_TXN[7:0]

9 FDI_TXP[7:0]

9 FDI_TXN[7:0]

9 FDI_TXP[7:0]

9 FDI_TXN[7:0]

9 FDI_TXP[7:0]

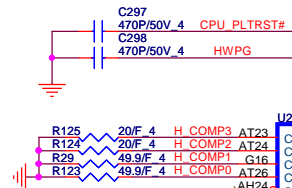
9 FDI_TXN[7:0]

9 FDI_TXP[7:0]

9 FDI_TXN[7:0]

9 FDI_TXP[7:0]

aitech1.ru



MISC

THERMAL

PWR MANAGEMENT

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

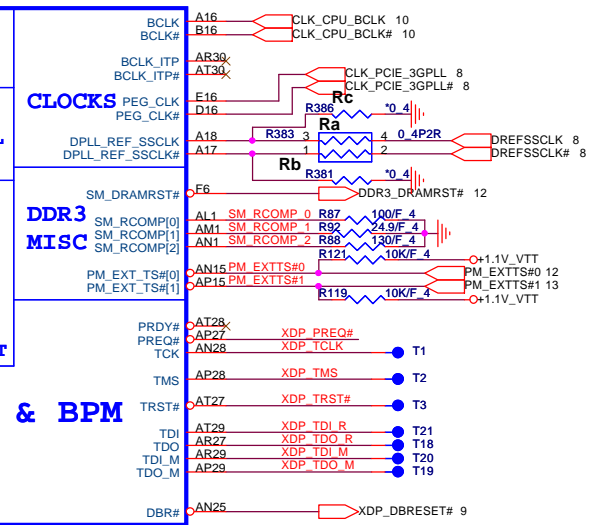
JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM



CLOCKS

DDR3

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

JTAG & BPM

U14

MC74VHC1G08DFT2G

23,31,35,36,37,39,40

HWP

H VTPWRGD

R162

2K/F_4

R163

1K/F_4

+1.1V_VTT

R80

976/F_4

R79

3K/F_4

1.1V

PM_DRAMPWRGD

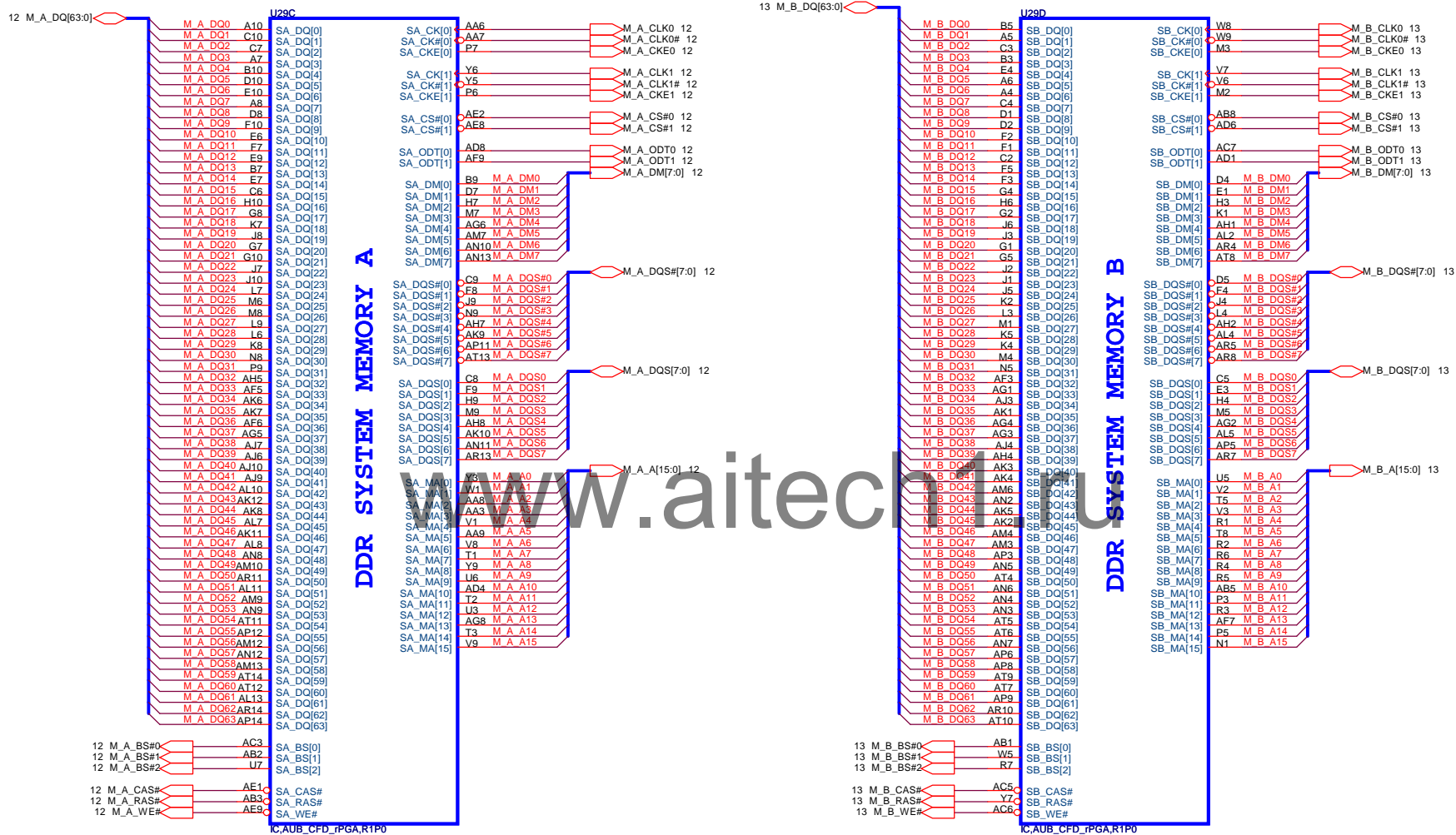
XDP TRST# R129 51.4



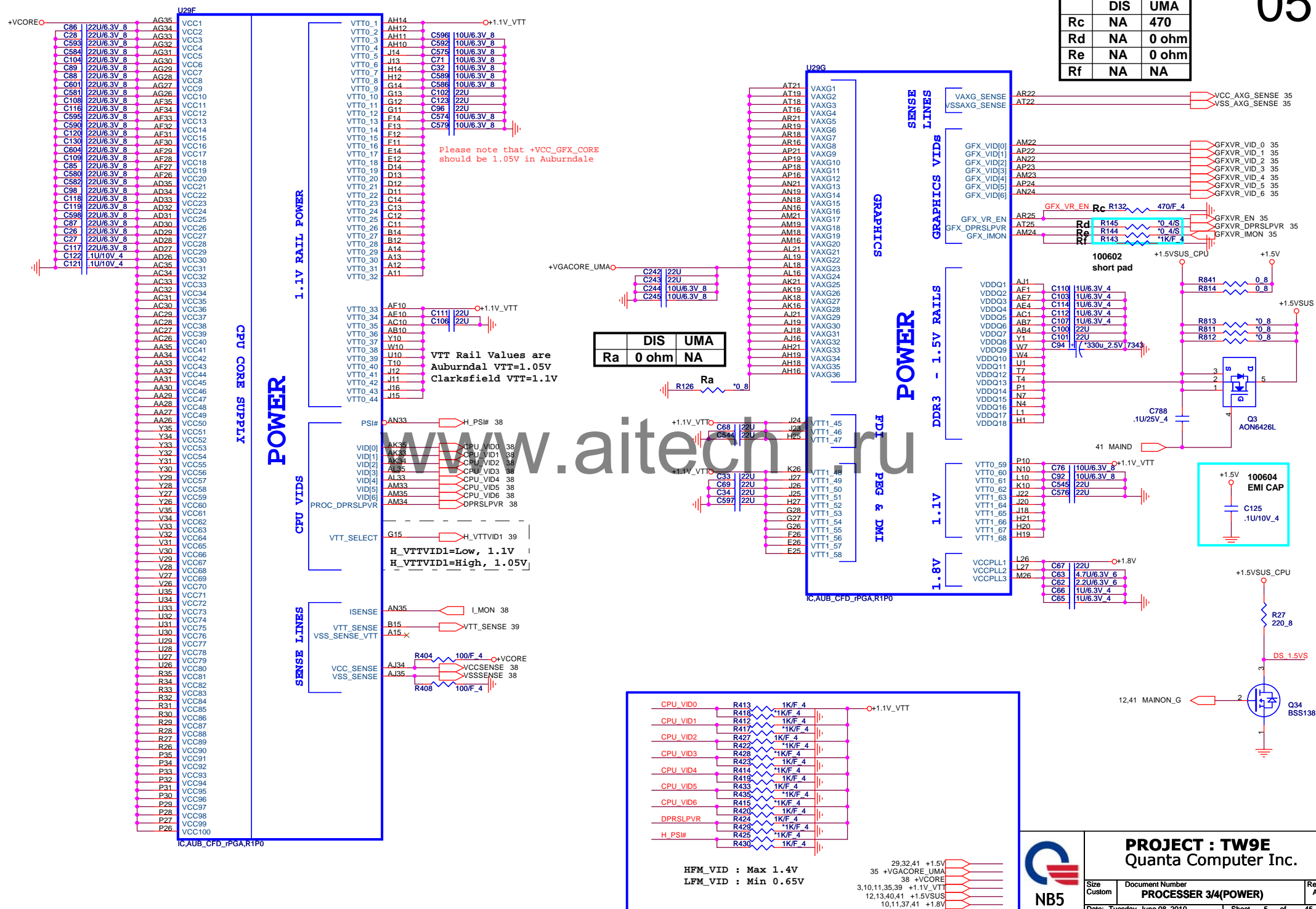
PROJECT : TW9E
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSOR 1/4(HOST&PEX)	A
Date:	Tuesday, June 08, 2010	Sheet 3 of 45

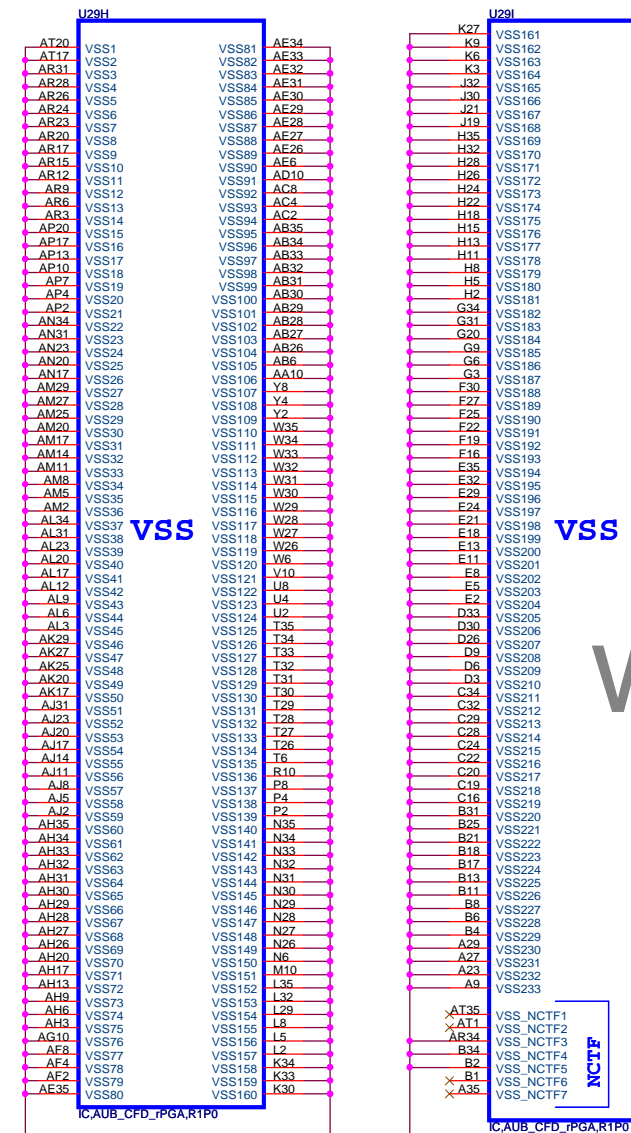
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



	DIS	UMA
Rc	NA	470
Rd	NA	0 ohr
Re	NA	0 ohr
Rf	NA	NA

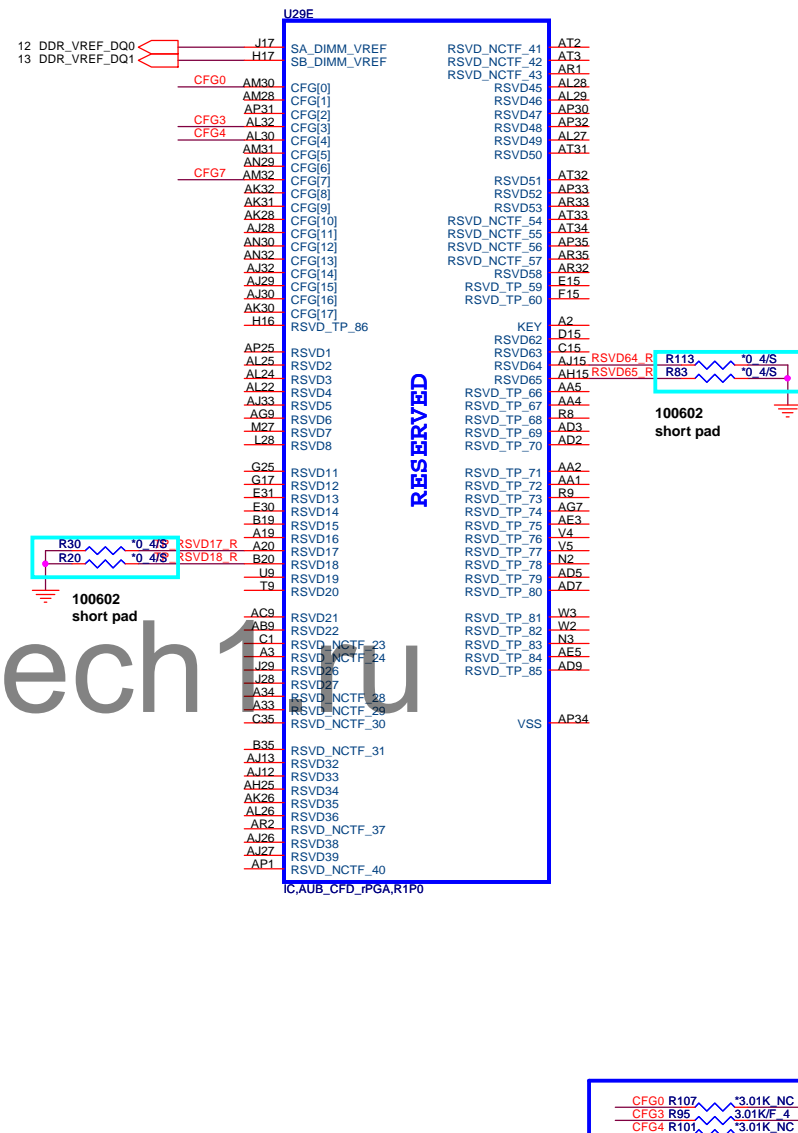


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01k \pm 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

For Discrete only

```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```

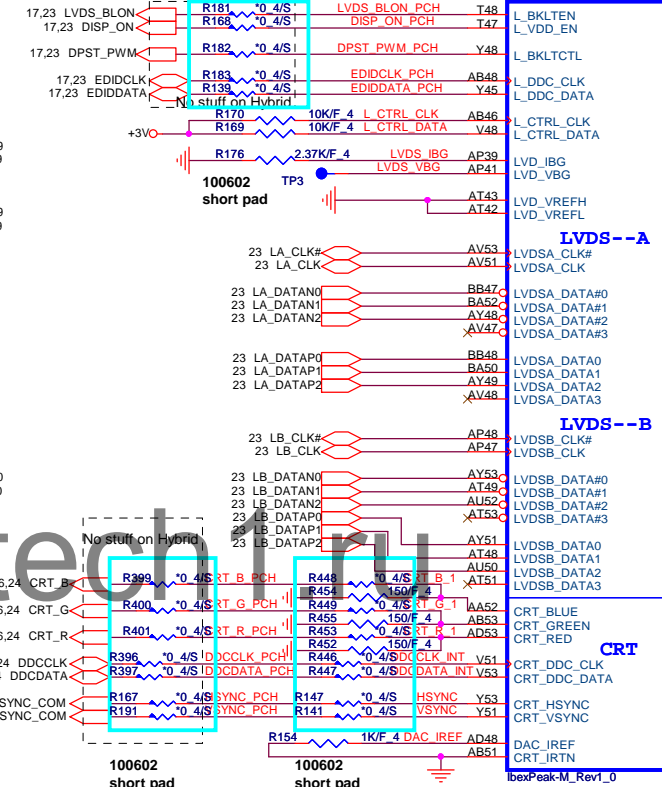


PROJECT : TW9E
Quanta Computer Inc.

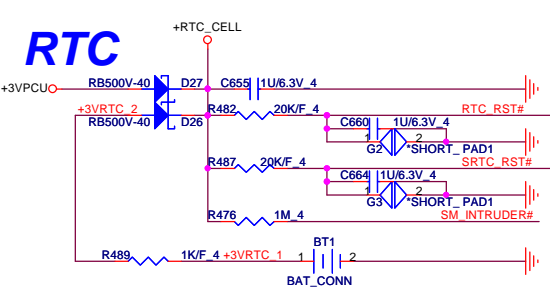
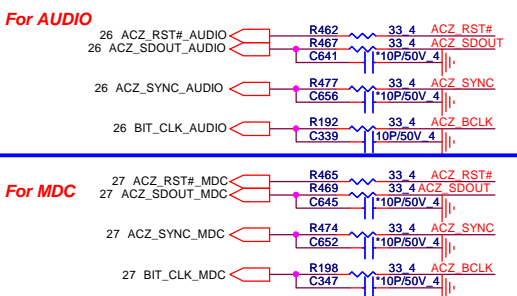
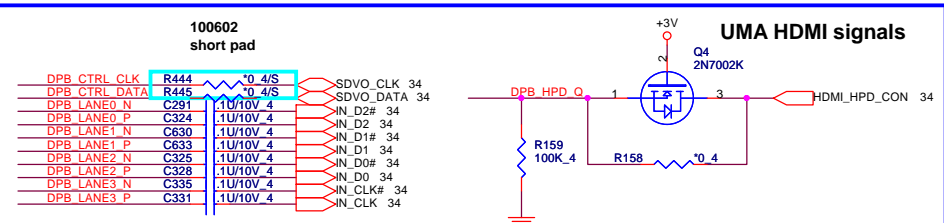
Size Custom	Document Number PROCESSER 4/4(GND)	Rev A
Date: Tuesday, June 08, 2010	Sheet 6 of 45	



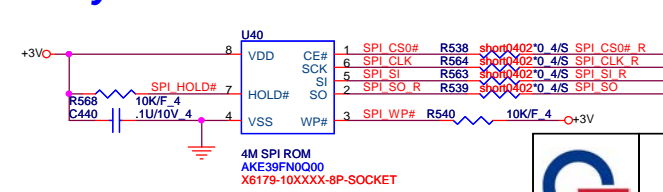
UMA and Hybird LVDS & CRT signals



1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.



4M byte SPI ROM for ME



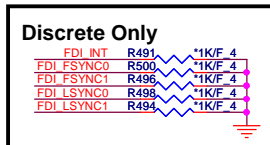
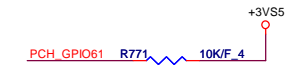
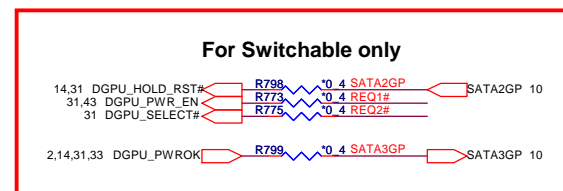
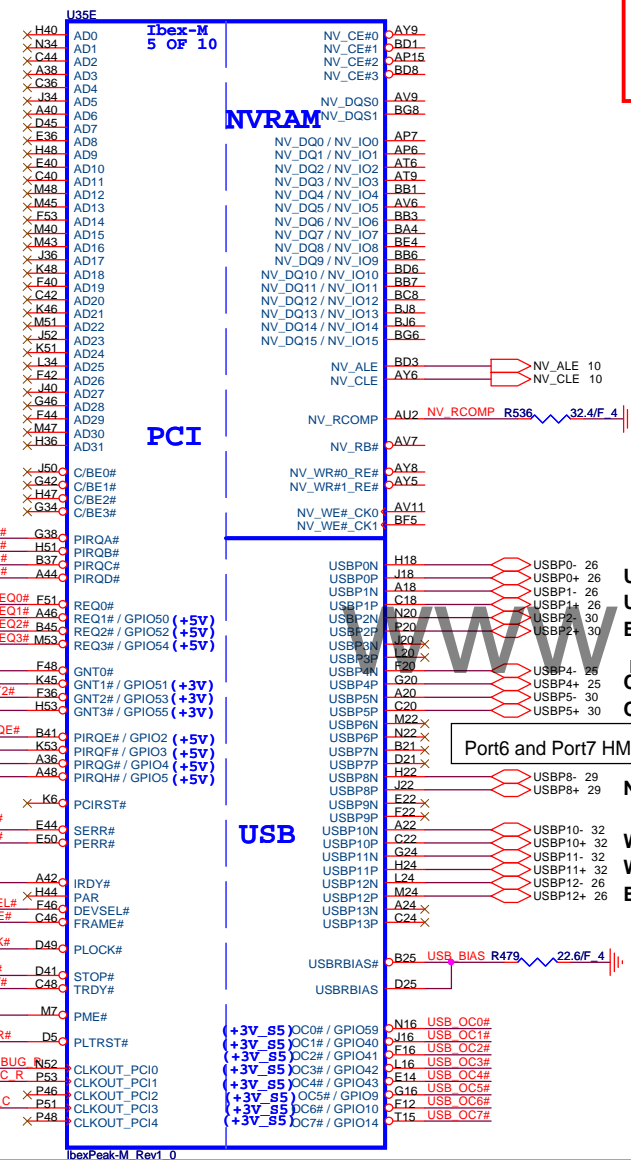
4M byte SPI ROM for ME
WINBOND: AKE391P0N00
EON: AKE39FN0Q00
Socket: DG008000031



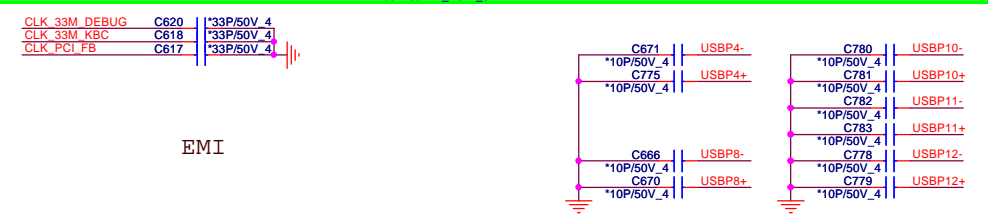
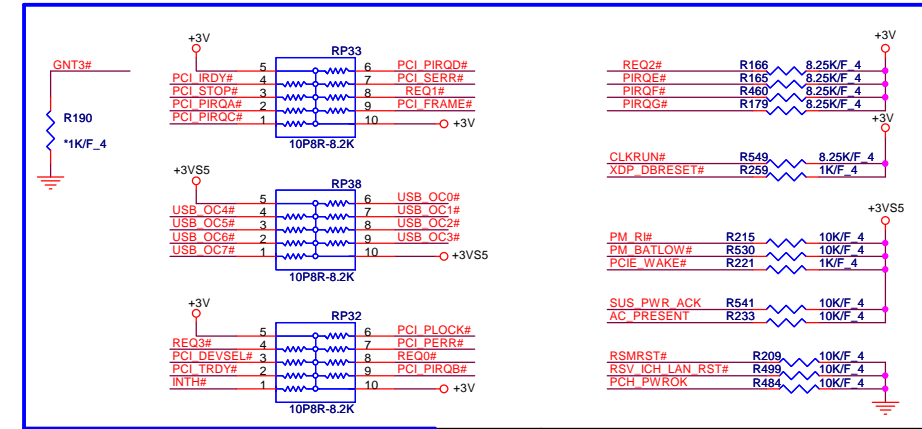
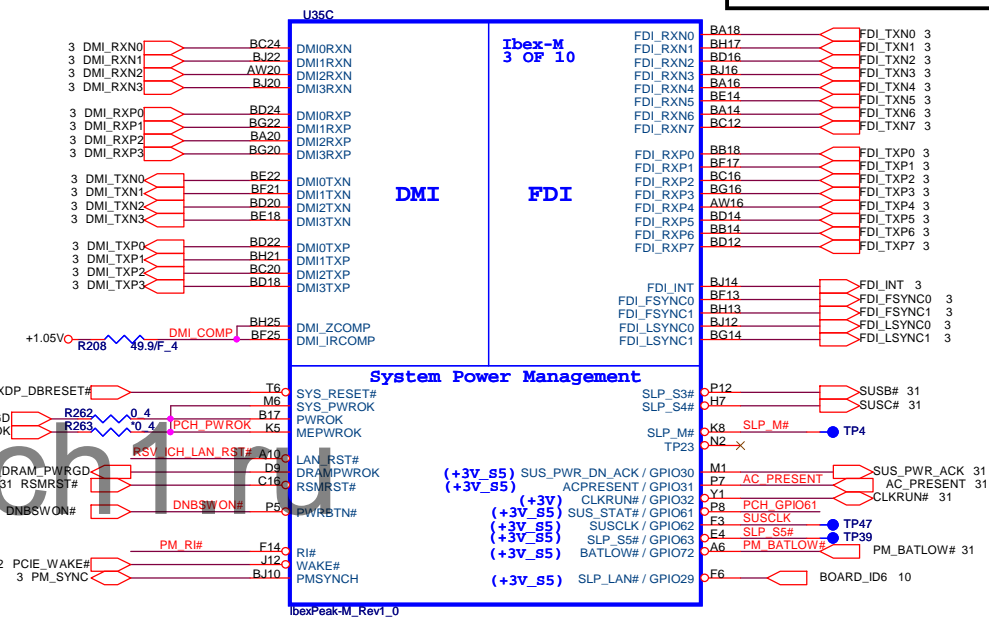
PROJECT : TW9E
Quanta Computer Inc.

Size Custom	Document Number PCH 1/5 (SATA,HDA,LPC)	Rev A
Date: Tuesday, June 08, 2010	Sheet 7 of	45

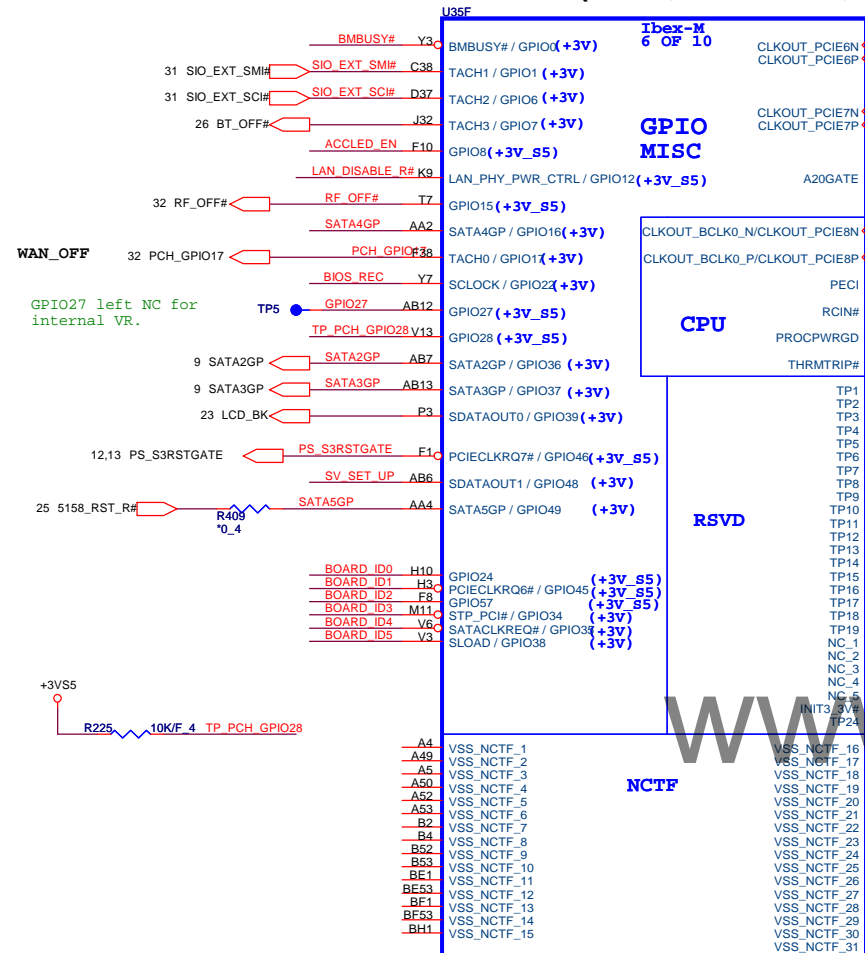
IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)



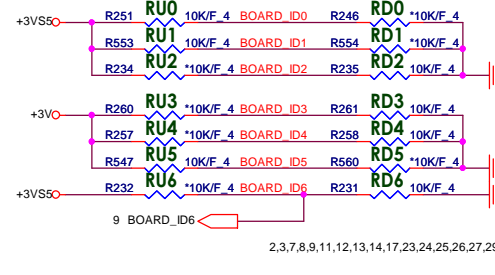
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



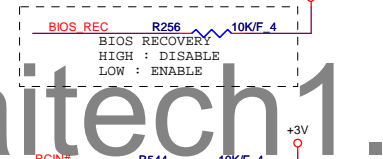
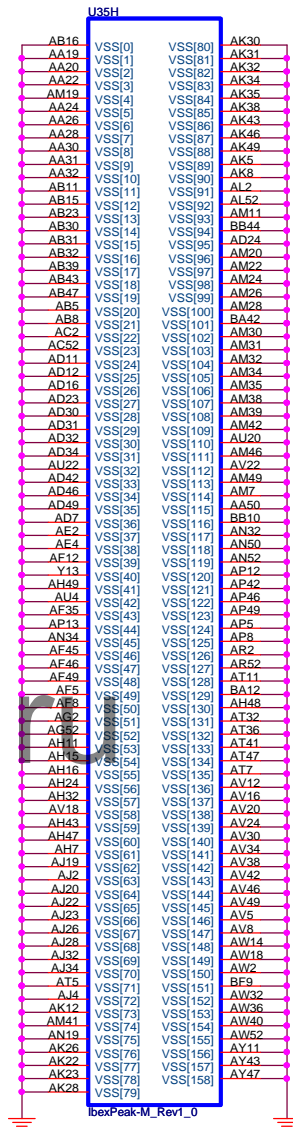
Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6" / 14"			0=QL4/TW9 1=QL2/SW9				
Switchable						1=YES 0=NO	

Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RDO (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RDO (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RDO (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

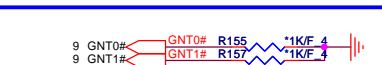
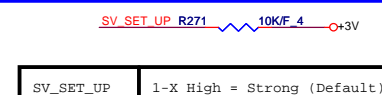
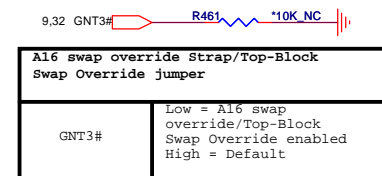
BOARD ID SETTING



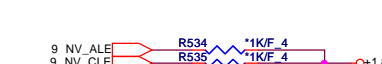
IBEX PEAK-M (GND)



10

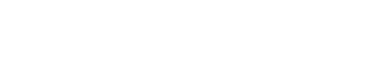
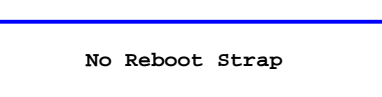


PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

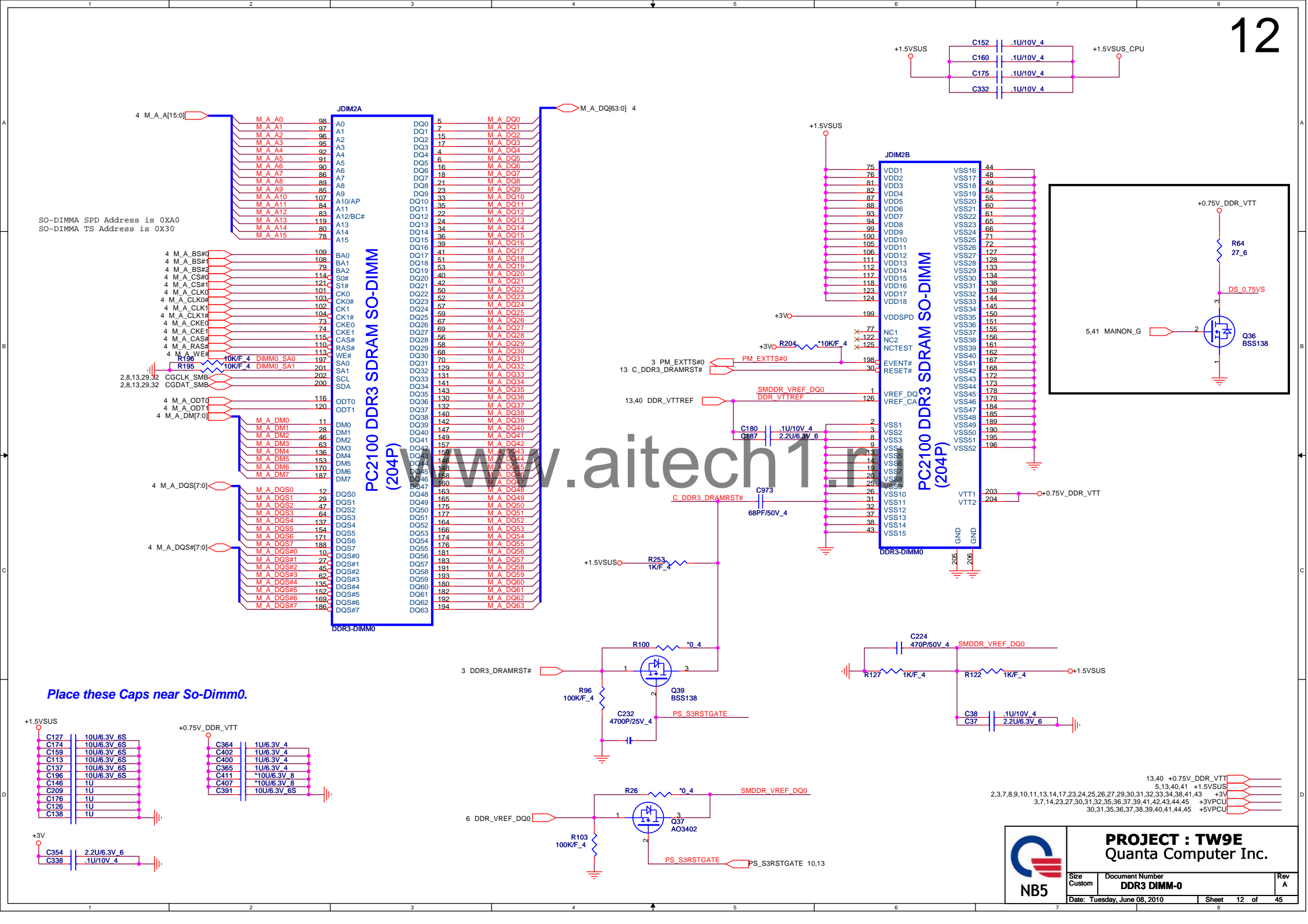
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

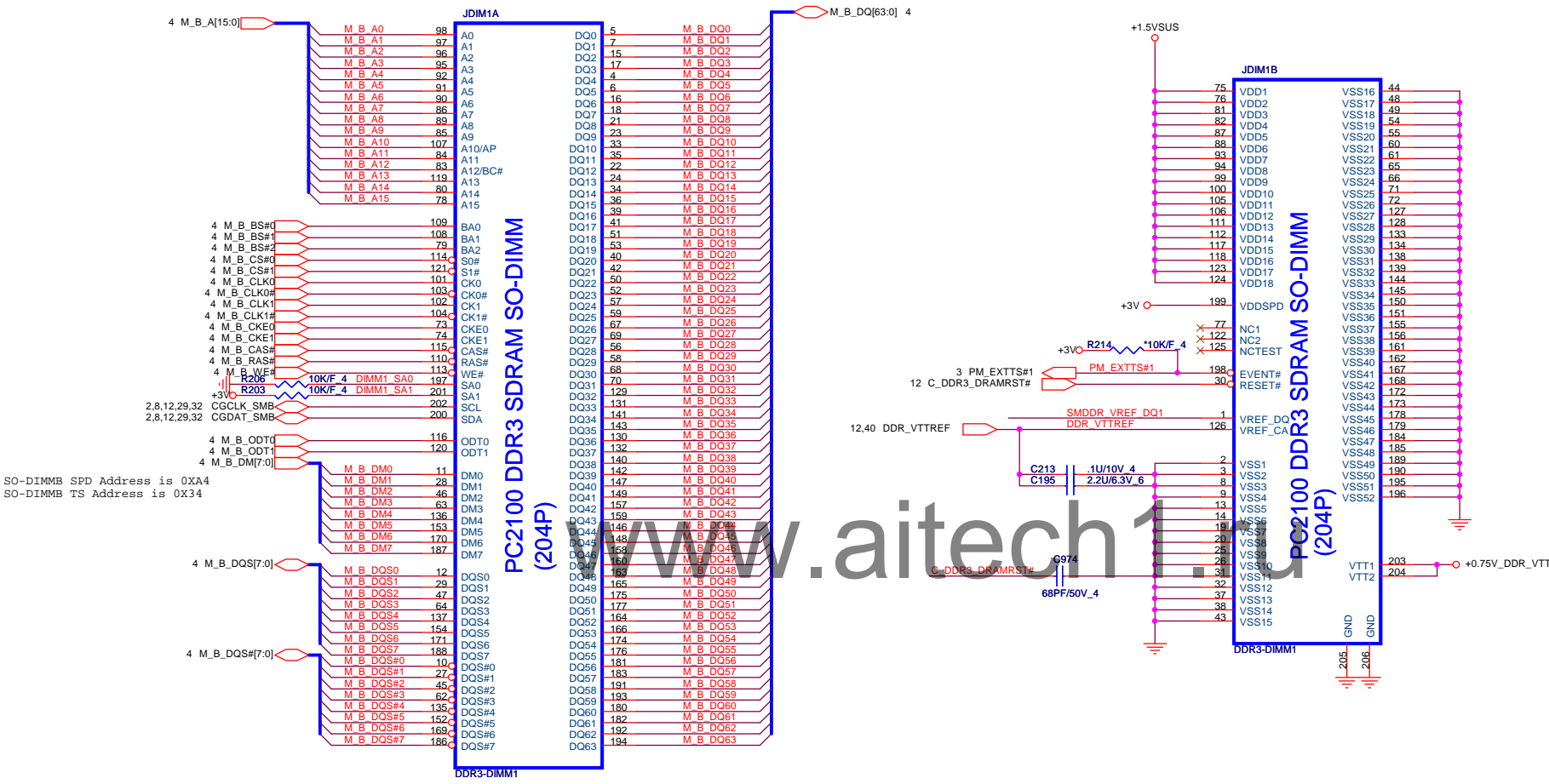


PROJECT : TW9E
Quanta Computer Inc.

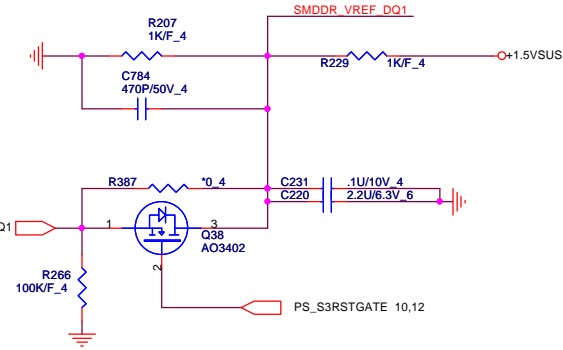
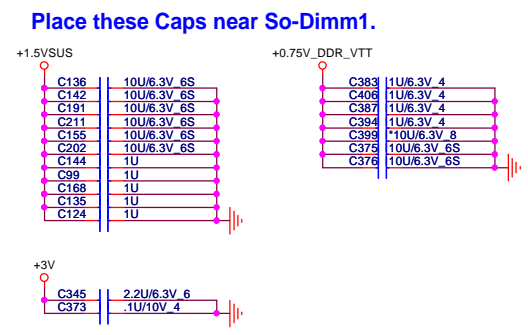
Size Custom	Document Number	Rev A
	PCH 4/5 (GPIO & Strap)	
Date: Monday, June 07, 2010	Sheet 10 of 45	





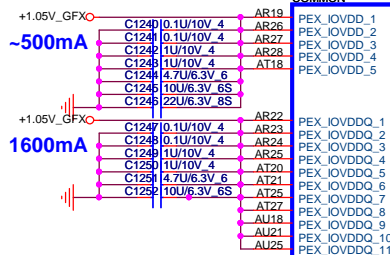


SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

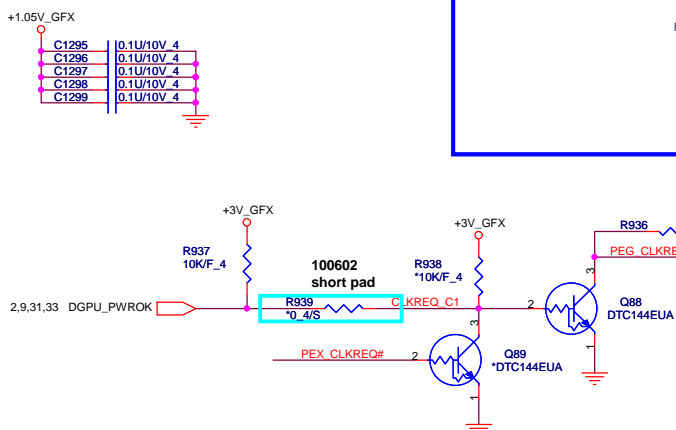
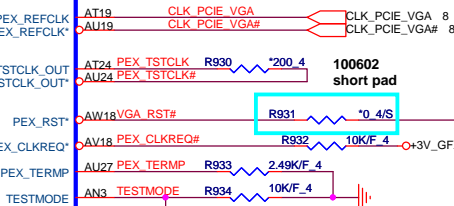
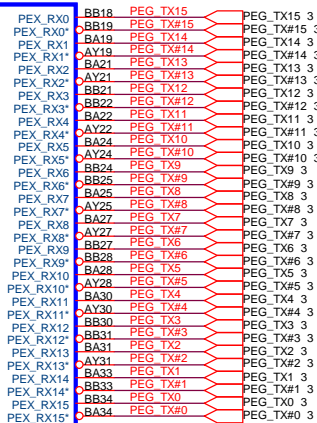


12,40 +0.75V_DDR_VTT
5,12,40,41 +1.5VSUS
2,3,7,8,9,10,11,12,14,17,23,24,25,26,27,29,30,31,32,33,34,38,41,43 +3V
3,7,14,23,27,30,31,32,35,36,37,39,41,42,43,44,45 +3VPCU
30,31,35,36,37,38,39,40,41,44,45 +5VPCU

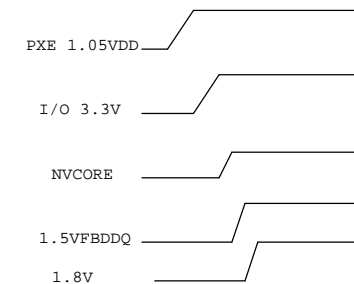
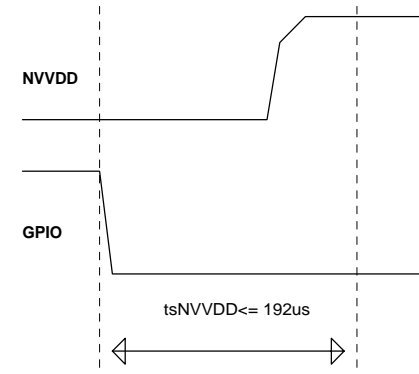
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

U77A
fcbga1328-nvidia-n11e
COMMON

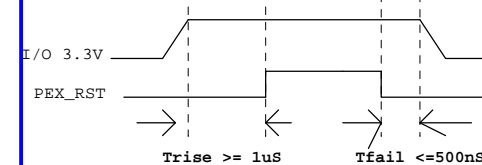
PCIEXPRESS

15,16,33,43 +1.05V_GFX
16,17,33,43 +3V_GFX
3,7,23,27,30,31,32,35,36,37,39,41,42,43,44,45 +3VPCU

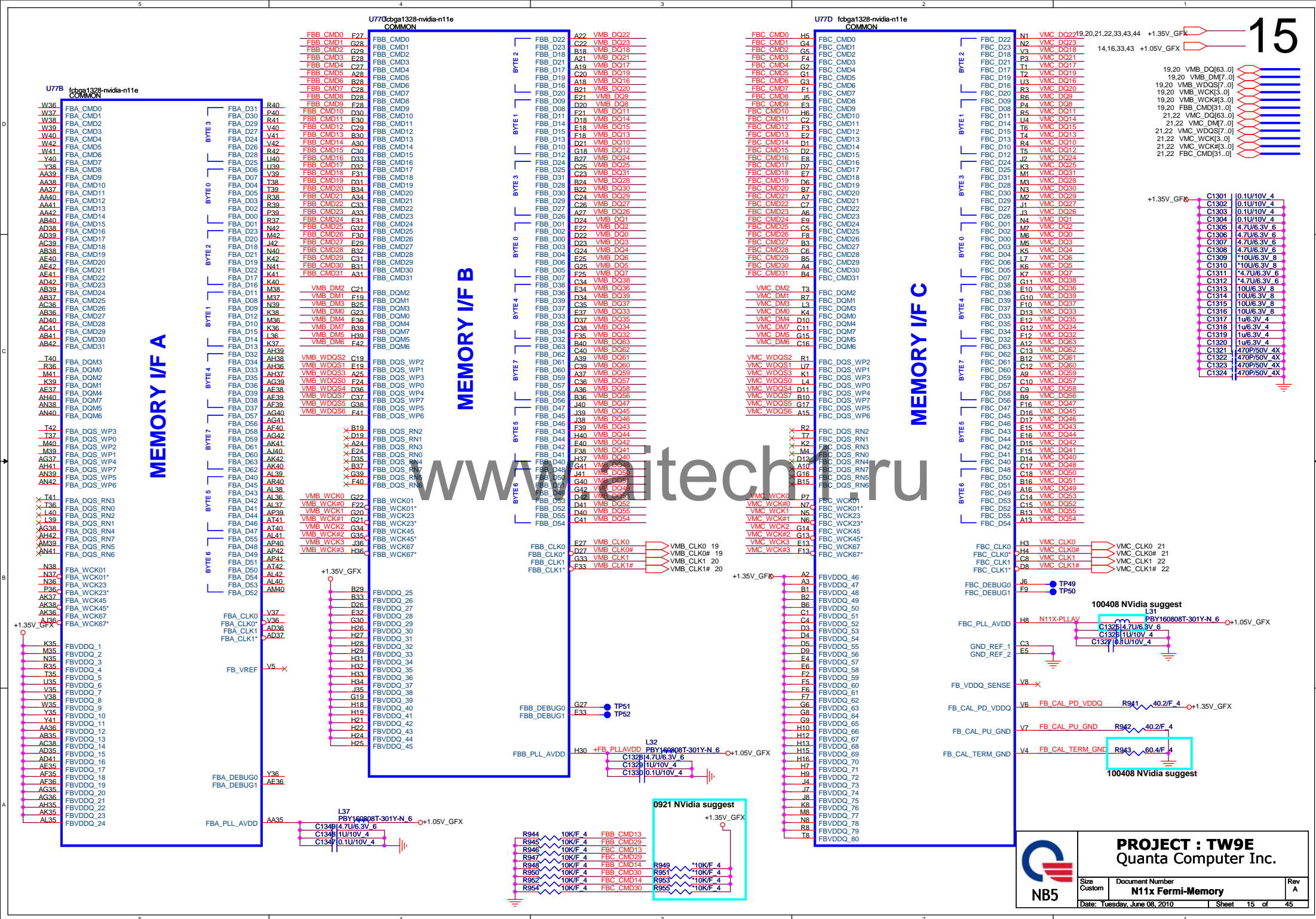
power up sequence

NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time

PEX_RST timing

PROJECT : TW9E
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N11x Fermi-PCIE	A
Date: Tuesday, June 08, 2010	Sheet 14 of 45	



U77E
fcbga1328-nvidia-n11e
COMMON

LVDS clk spread : Center
+/-0.5% (30~33KHZ)

100414 NVidia suggest
Optimus 1.0
10K pull down



IFPAB(LVDS)

- IFPA_TXC
- IFPA_TXC*
- IFPA_TXD0
- IFPA_TXD0*
- IFPA_TXD1
- IFPA_TXD1*
- IFPA_TXD2
- IFPA_TXD2*
- IFPA_TXD3
- IFPA_TXD3*
- IFPB_TXC
- IFPB_TXC*
- IFPB_TXD4
- IFPB_TXD4*
- IFPB_TXD5
- IFPB_TXD5*
- IFPB_TXD6
- IFPB_TXD6*
- IFPB_TXD7
- IFPB_TXD7*

- AV13
- AW13
- AU10
- AT10
- AV10
- AW10
- AV11
- AW11
- AV12
- AW12
- BA18
- AY18
- AX13
- BA13
- AY15
- BA15
- BB16
- SB15
- BA16
- AY16

+IFPCD_PLLVDD AN8

+IFPCD_IOVDD AM8

IFPCD_RSET AU8

IFPC

- IFPC_AUX_N / I2CW_SDA
- IFPC_AUX / I2CW_SCL
- IFPC_L3_N
- IFPC_L3
- IFPC_L2_N
- IFPC_L2
- IFPC_L1_N
- IFPC_L1
- IFPC_L0_N
- IFPC_L0

- AU6
- AV6
- AU7
- AV7
- AW6
- AW7
- AV8
- AW8
- AW9
- AV9

+3V_GFX R958 10K 4 CEC AJ3

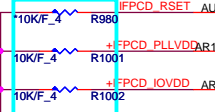
IFPD

- IFPD_AUX_N / I2CX_SDA
- IFPD_AUX / I2CX_SCL
- IFPD_L3_N
- IFPD_L3
- IFPD_L2_N
- IFPD_L2
- IFPD_L1_N
- IFPD_L1
- IFPD_L0_N
- IFPD_L0

- AV3
- AW3
- BB9
- BB10
- BA10
- AY10
- BA12
- AY12
- BB12
- BB13

TMDs channel two

100408 NVidia suggest



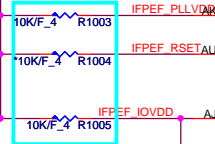
IFPD

- IFPE_AUX / I2CY_SCL
- IFPE_AUX_N / I2CY_SDA
- IFPE_L0
- IFPE_L0*
- IFPE_L1
- IFPE_L1*
- IFPE_L2
- IFPE_L2*
- IFPE_L3
- IFPE_L3*
- IFPF_AUX / I2CZ_SCL
- IFPF_AUX_N / I2CZ_SDA
- IFPF_L0
- IFPF_L0*
- IFPF_L1
- IFPF_L1*
- IFPF_L2
- IFPF_L2*
- IFPF_L3
- IFPF_L3*

- BA3
- AY2
- AW5
- AY5
- AY4
- AW4
- AW2
- AY3
- BA5
- BA7
- AY7
- BB7
- BB6
- BA6
- AY6

Display port output

100408 NVidia suggest

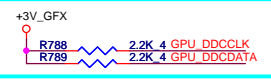
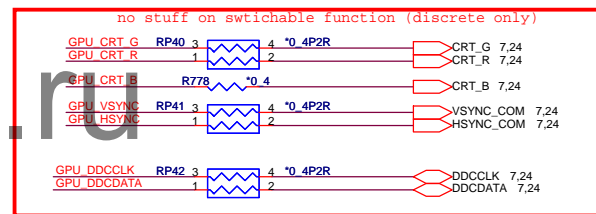


IFPEF

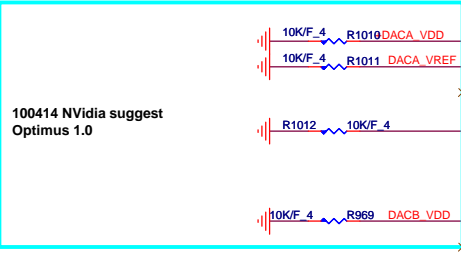
- IFPE_AUX / I2CY_SCL
- IFPE_AUX_N / I2CY_SDA
- IFPE_L0
- IFPE_L0*
- IFPE_L1
- IFPE_L1*
- IFPE_L2
- IFPE_L2*
- IFPE_L3
- IFPE_L3*
- IFPF_AUX / I2CZ_SCL
- IFPF_AUX_N / I2CZ_SDA
- IFPF_L0
- IFPF_L0*
- IFPF_L1
- IFPF_L1*
- IFPF_L2
- IFPF_L2*
- IFPF_L3
- IFPF_L3*

- BA3
- AY2
- AW5
- AY5
- AY4
- AW4
- AW2
- AY3
- BA5
- BA7
- AY7
- BB7
- BB6
- BA6
- AY6

Optimus unstuff
For RGB , HSYNC, VSYNC resistor



100414 NVidia suggest
2.2K pull-high



DAC A (CRT)

- DACA_RED
- DACA_GREEN
- DACA_BLUE
- DACA_RSET
- DACA_HSYNC
- DACA_VSYNC
- I2CA_SCL
- I2CA_SDA

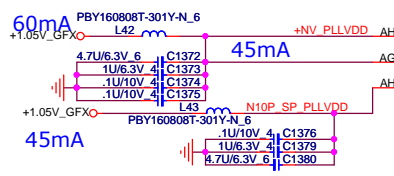
- AW17 GPU CRT R
- AY17 GPU CRT G
- AW16 GPU CRT B
- AU16 CRT HSYNC
- AV16 CRT VSYNC
- AK2
- AK1

DAC B

- DACB_RED
- DACB_GREEN
- DACB_BLUE
- DACB_RSET
- DACB_HSYNC
- DACB_VSYNC
- I2CB_SCL
- I2CB_SDA

- AW15
- AY14
- AW14
- AY15
- AU15

10 kΩ pull-down only if no spread chip used.



XTAL_PLL

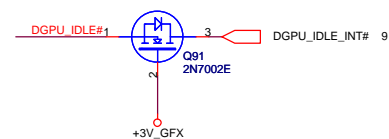
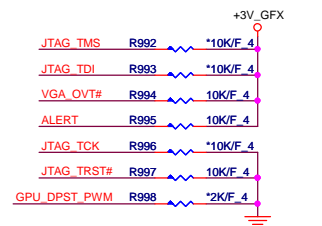
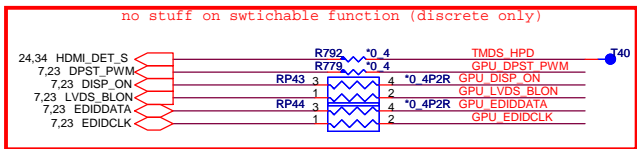
- XTAL_SIN
- XTAL_OUTBUFF
- XTAL_IN
- XTAL_OUT

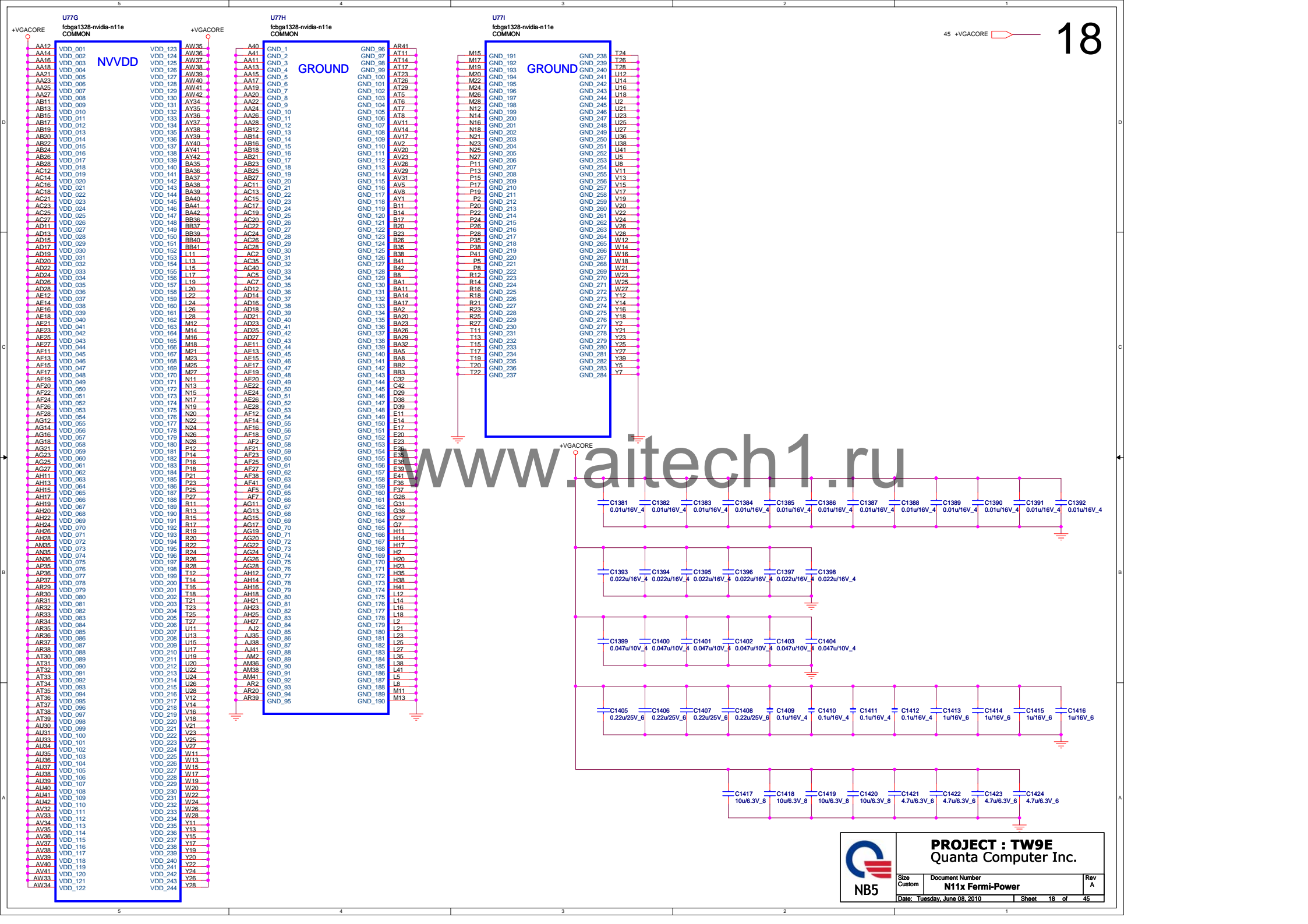
- AU4 XTAL SSIN
- AU1 XTAL OUT
- AU2 XTALIN
- AU3 XTALOUT

PLACE CLOSE TO DGUP

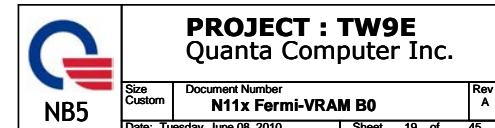
STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

Optimus:
Sutff : Y8 , C1100 , C1101, R711
un-stuff : R709 , R712

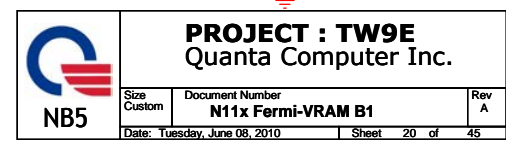




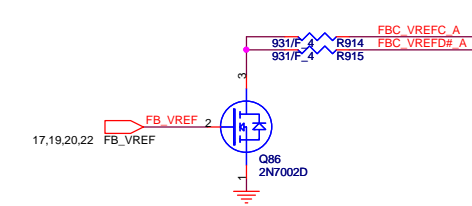
19



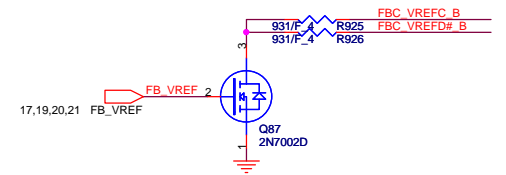
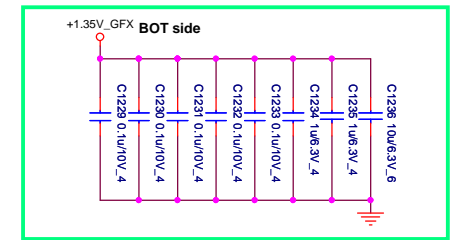
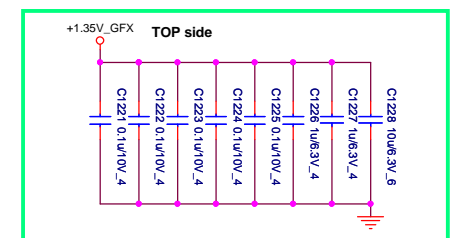
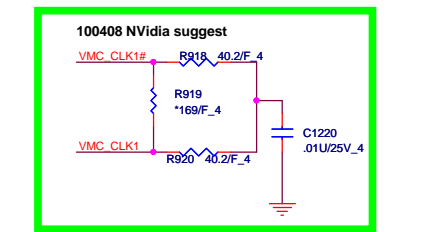
20



21

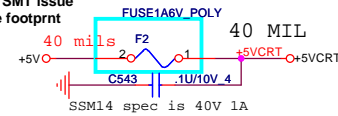


22

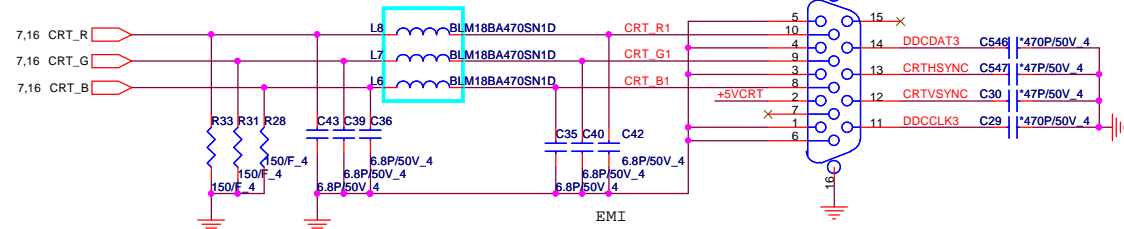


1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B
-
- 3/30 Del Location RP2,RP4,RP6,RP8,RP10,RP12,RP14,RP16 OPTION SIGNAL FROM NB FOR UMA VGA
-
- 3/30 Del Location RP7,RP1,RP3,RP5,RP15,RP9,RP11,RP13 : OPTION SIGNAL FROM Nvidia to VGA
-

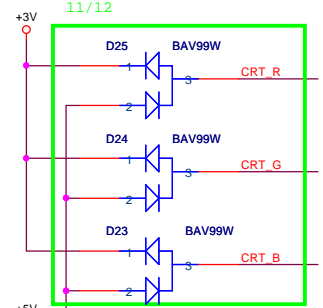
100527 SMT issue
Change footprint



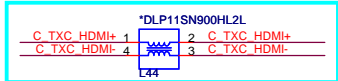
100607 CRT interface
Change to BLM18BA470SN1D



CRT PORT

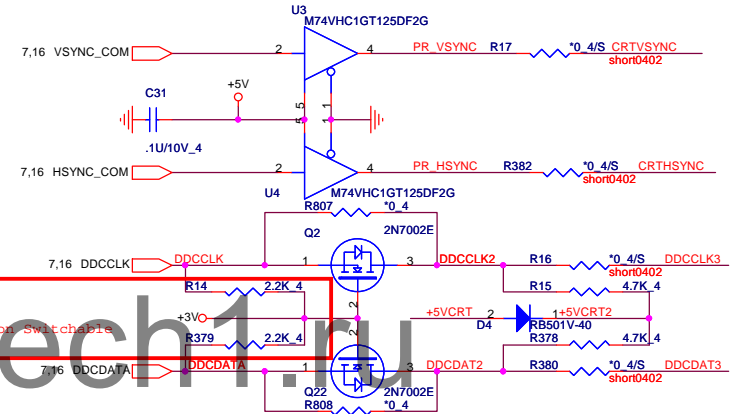
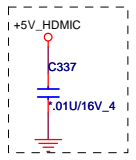
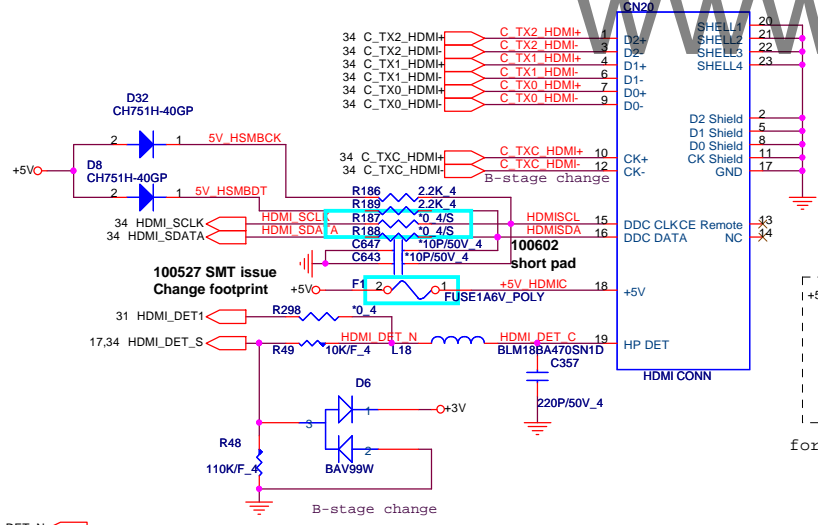


100602
For EMI



HDMI PORT

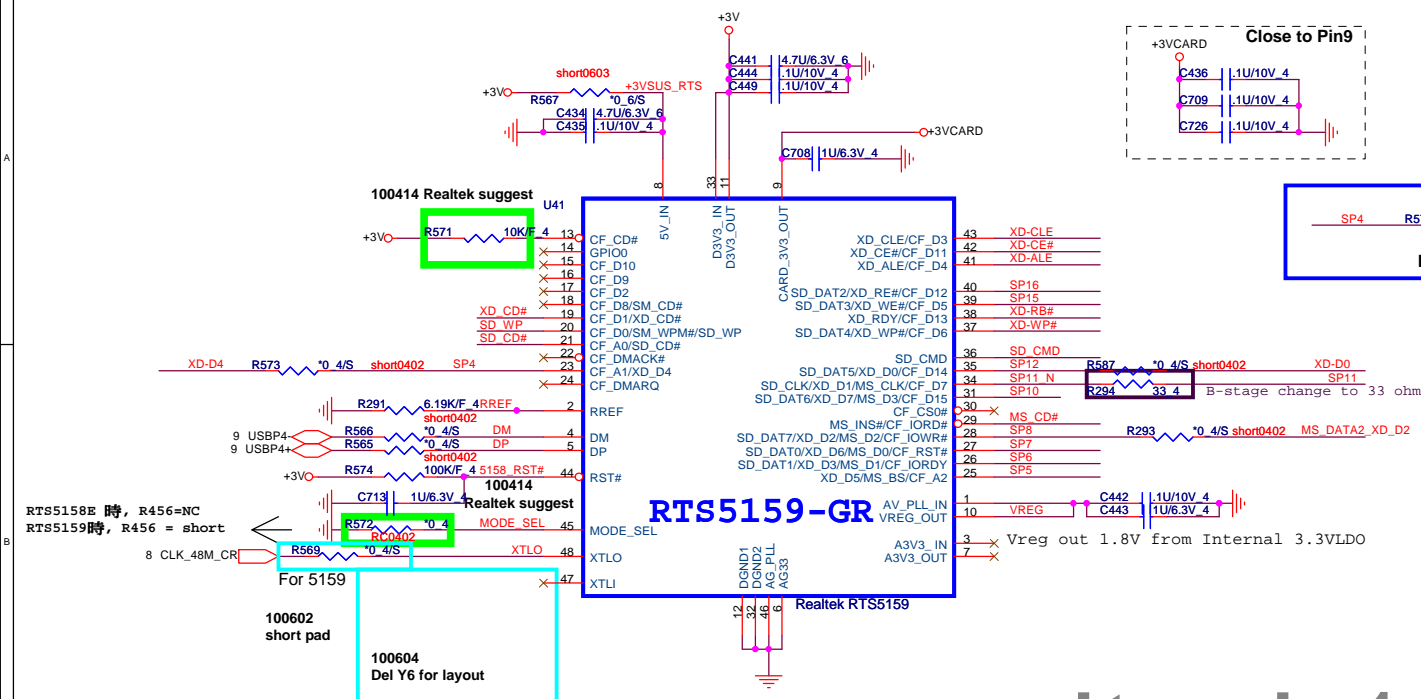
UMA only
Not Mount on Switchable



4/7 DEL Only for Discrete and Hybrid

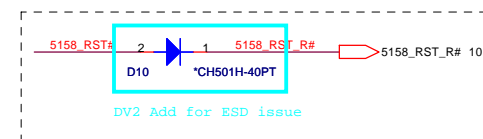
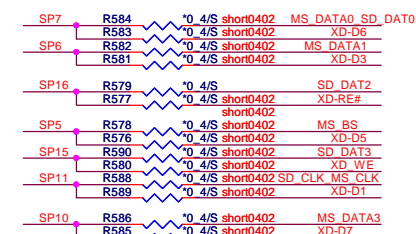
R187 / R188 for Switchable / UMA

Note:



	SD/MMC	MS	XD
SP0			
SP1			XD CD#
SP2	SD WP		
SP3	SD CD#		
SP4	SD DAT1		
SP5		MS BS	XD D4
SP6		MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK#	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4		XD WP#
SP14			XD R/B#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE

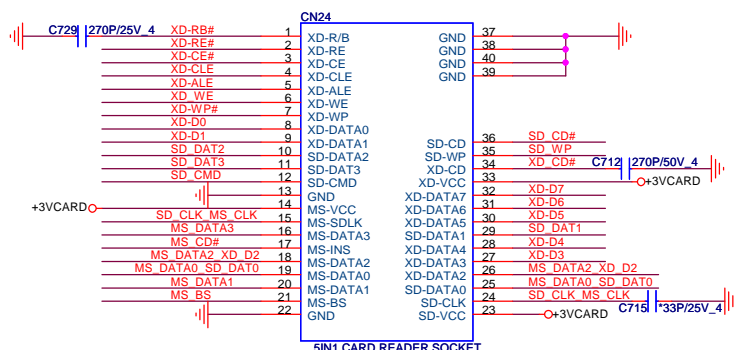
For RTS5159



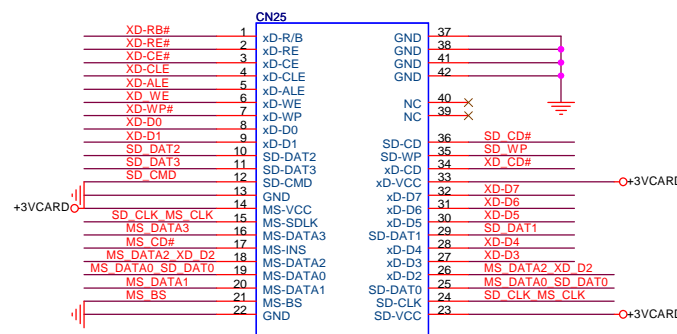
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5 IN1 CARD READER
XD,MMC/SD,MS/MSP

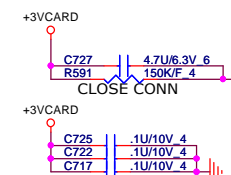
DV2 add 2'nd source



PV change footprint



*TAI TWUM 5IN1 CARD READER SOCKET
PV change footprint



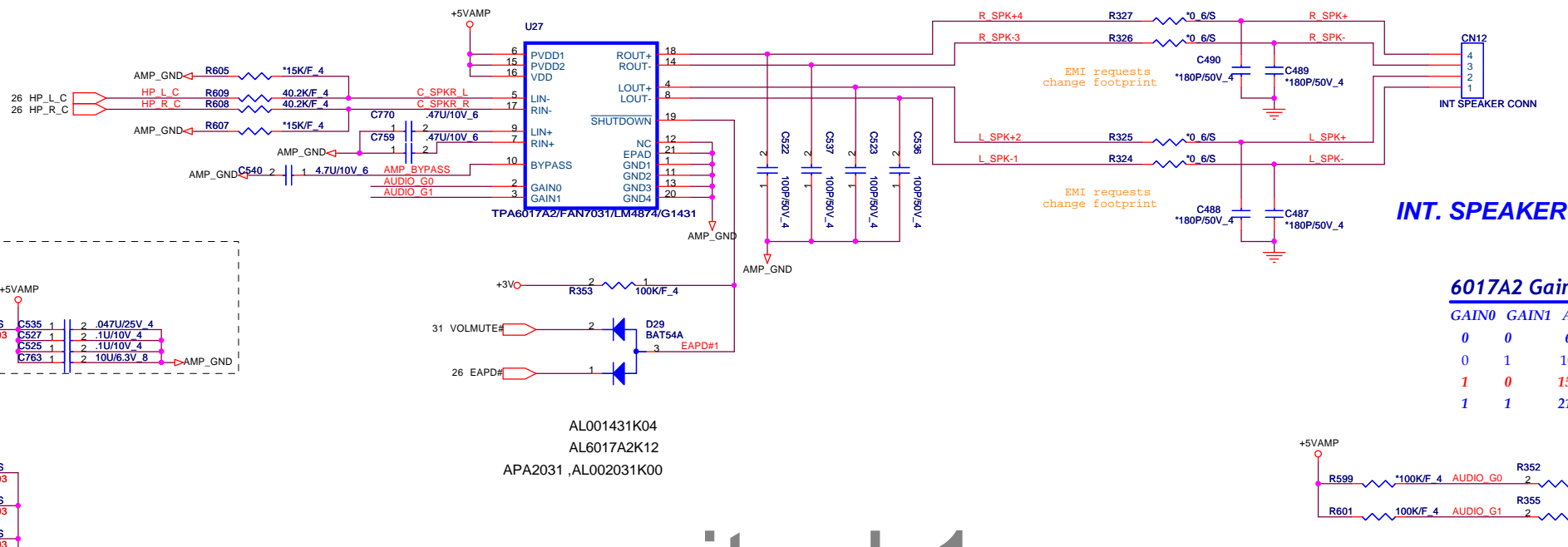
PROJECT : TW9E
Quanta Computer Inc.

Size	Document Number
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Custom	RTS5159 & CR SOCKET	A
Date: Tuesday, June 08, 2010	Sheet 25 of 45	

AUDIO AMPLIFIER

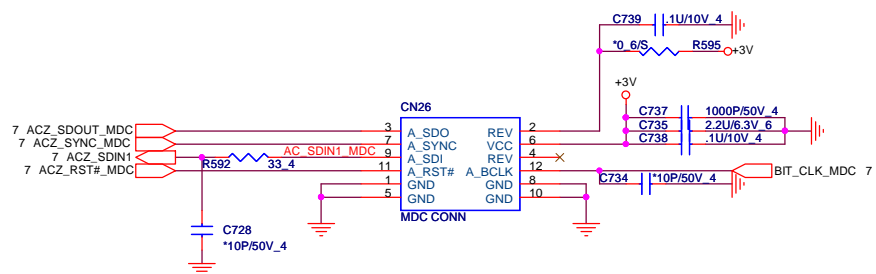
27



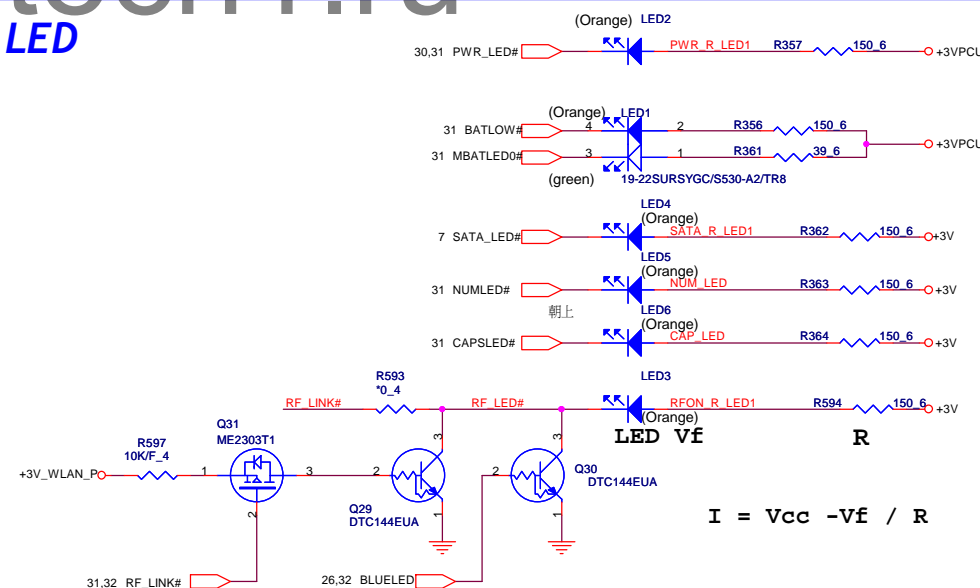
6017A2 Gain Table

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

MDC CONNECTOR



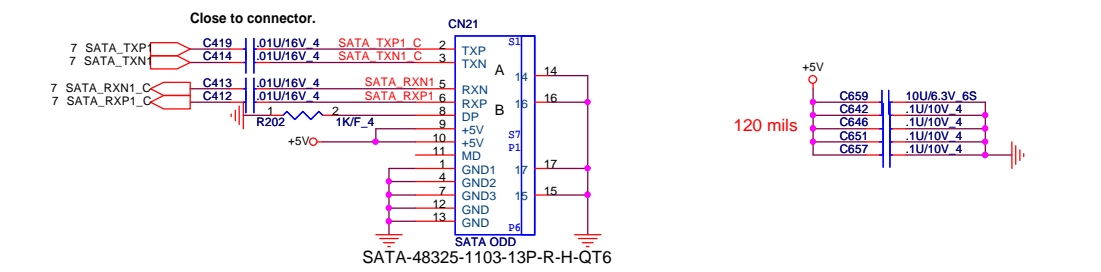
LED



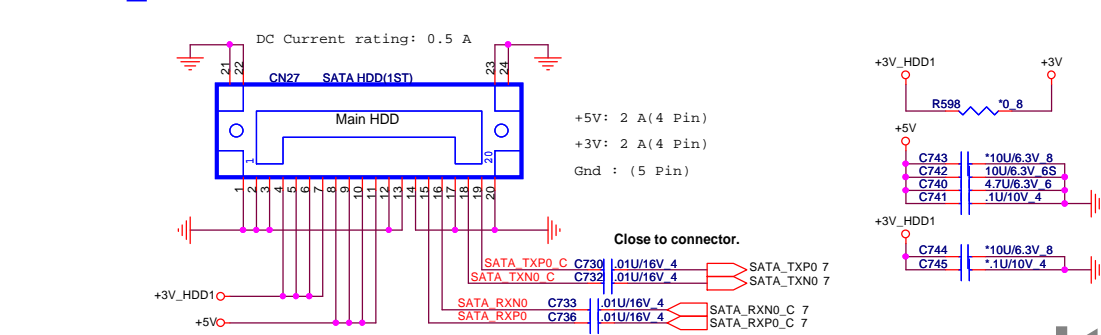
$$I = \frac{V_{cc} - V_f}{R}$$

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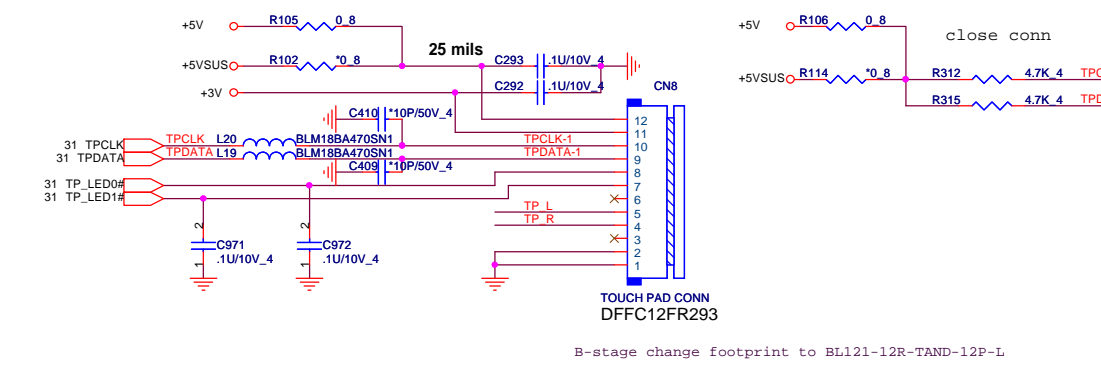
SATA ODD



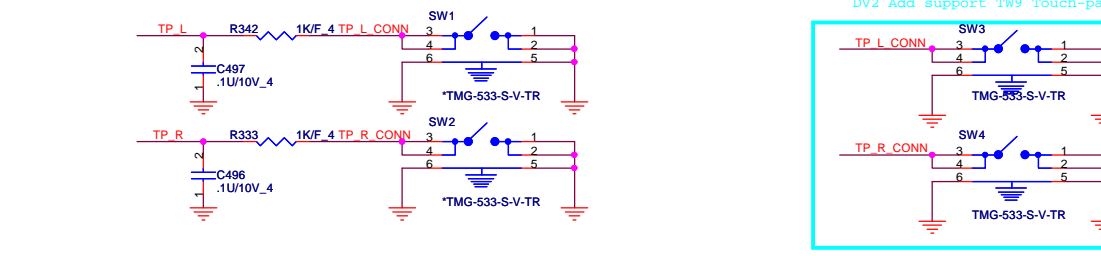
SATA_1 CONNECTOR



TOUCH PAD CONNECTOR

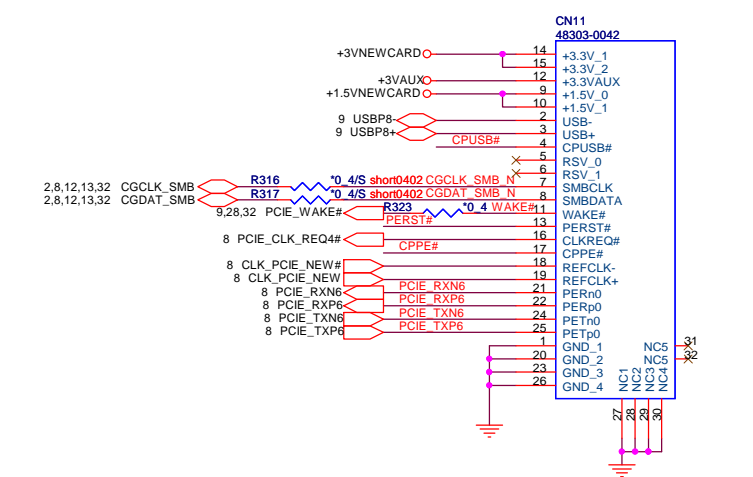


TOUCH PAD L/R SW1,SW2 in QL4 use, SW3,SW4 in TW9 use

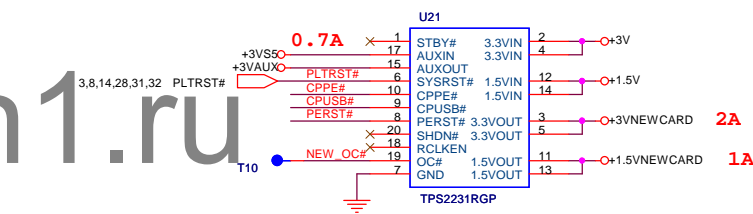


NEWCARD

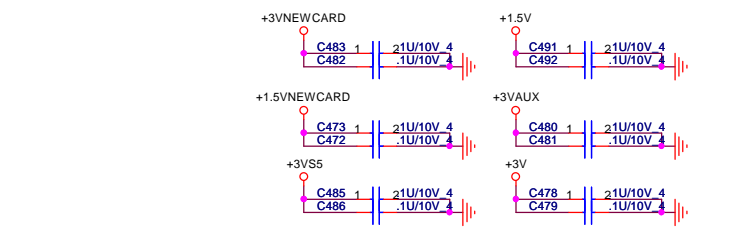
NEWCARD (PCIEXPRESS*1 + USB*1)




Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-1-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



Change net name from 3V_NEWCAUX to 3VAUX



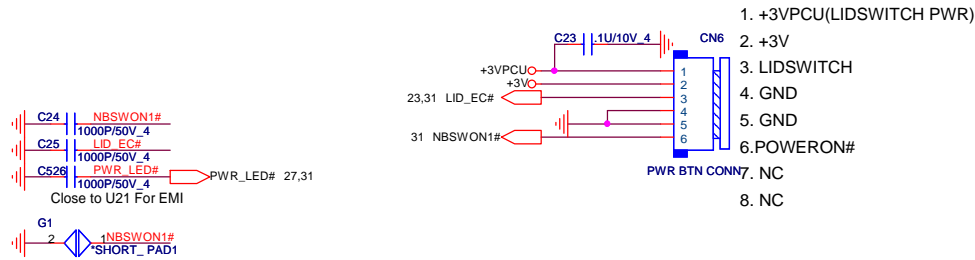


PROJECT : TW9E
Quanta Computer Inc.

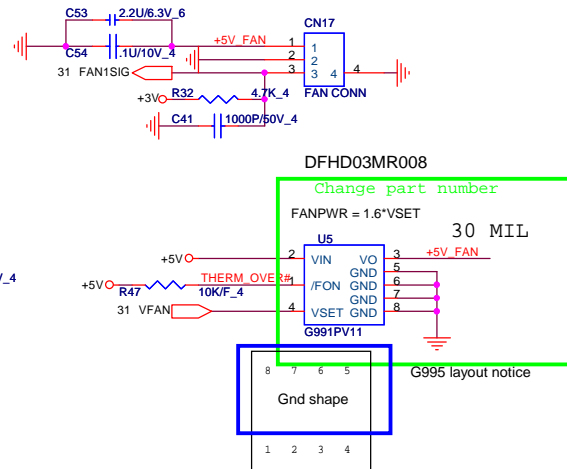
Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD/TP	A

Date: Monday, June 07, 2010 Sheet 29 of 45

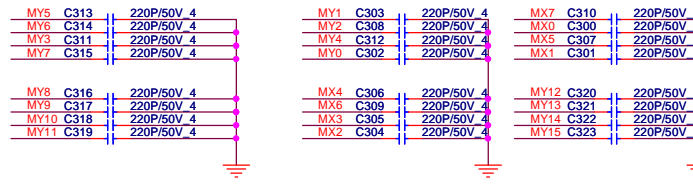
POWER BOTTON CONNECT



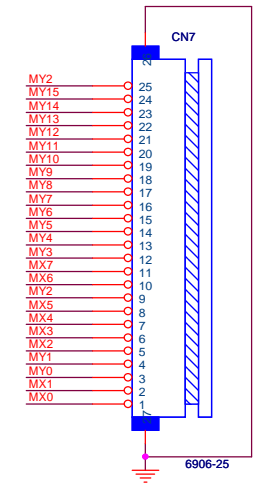
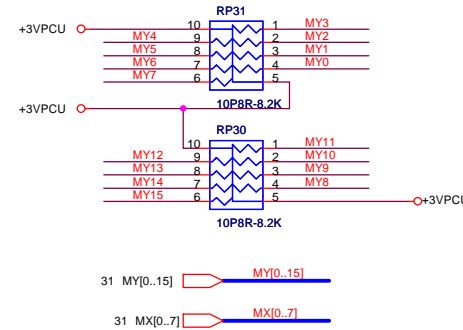
CPU FAN



KEYBOARD Con.

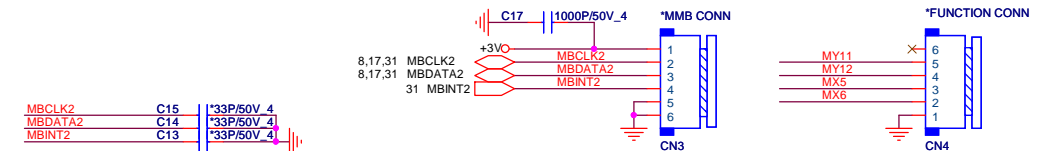


KEYBOARD PULL-UP

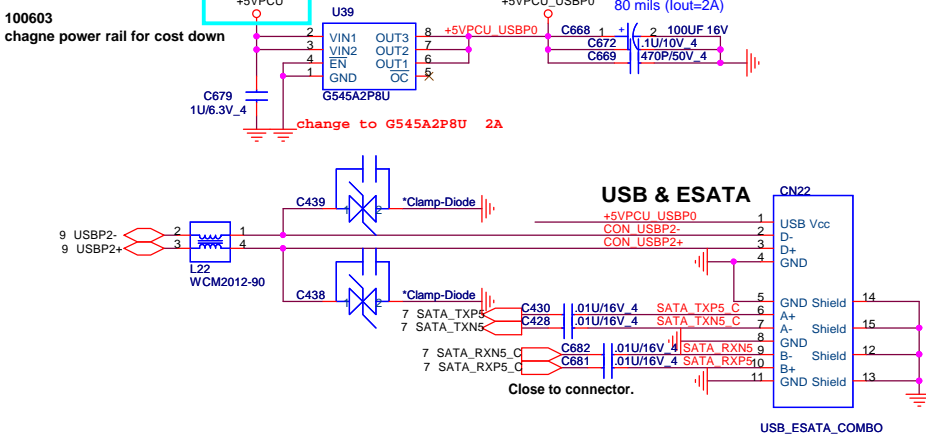


30

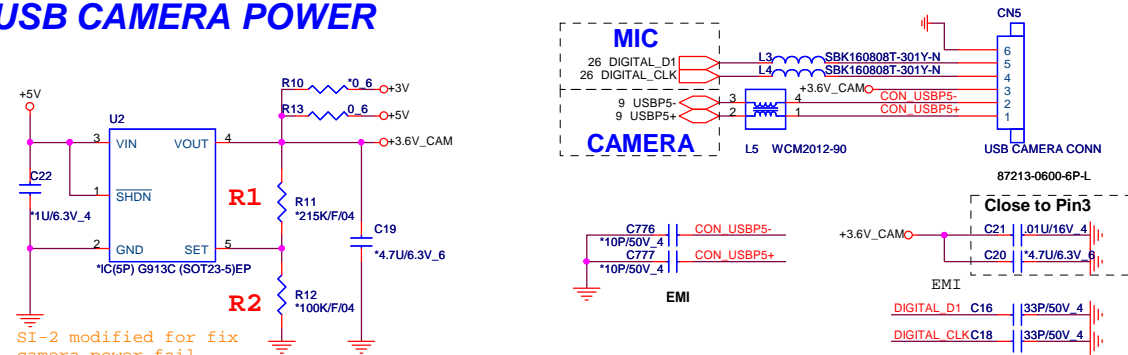
Capacity board Con.



E-SATA/USB COMBO



USB CAMERA POWER



SI-2 modified for fix camera power fail

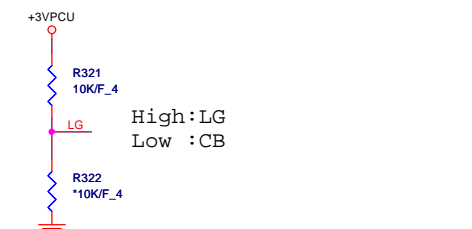
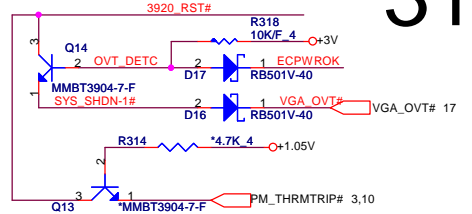
$$V_{out} = 1.25 (1 + R1/R2)$$



PROJECT : TW9E
Quanta Computer Inc.

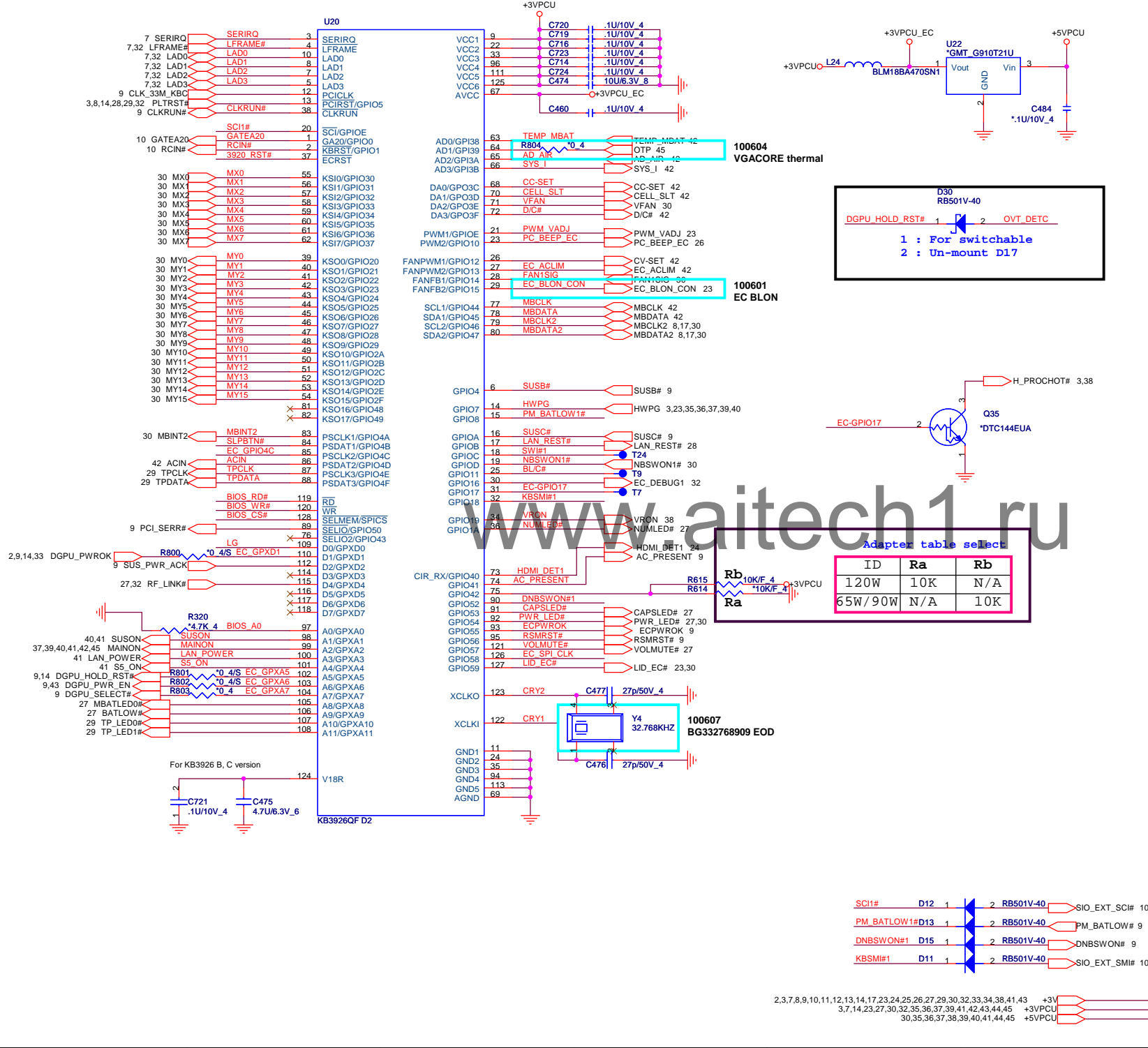
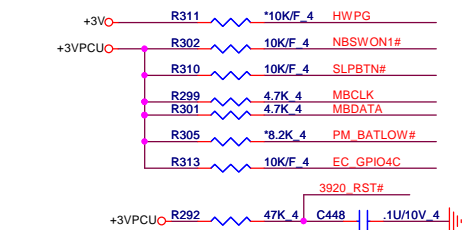
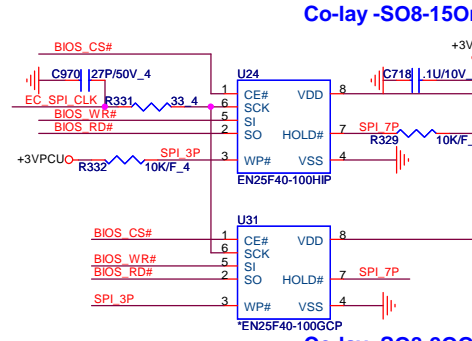
Size	Document Number	Rev
Custom	KB/PWR/ESATA/FAN/CAM/MIC	A
Date: Tuesday, June 08, 2010	Sheet 30 of 45	

thermal shutdown circuit



SPI BIOS
512K byte SPI ROM for EC

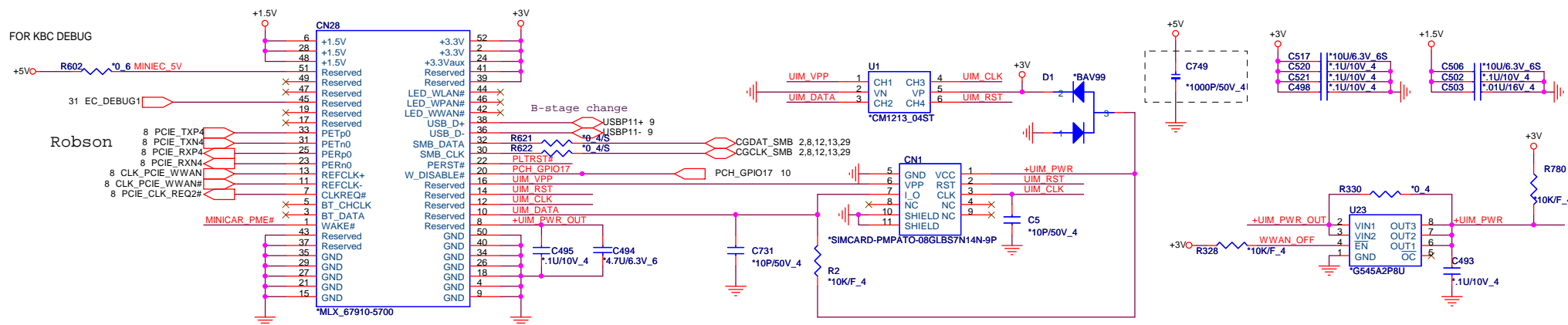
WINBOND: AKE37FN0N01, W25X40BVSSIG(SOIC)
EON: AKE372N0Q01, EN25F40-100HIP(SOIC)
Socket: DG008000031



32



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DGPU_Channel-A/B

3/30 Del Location U38 : LVDS Channel Switch

To LVDS Conn.

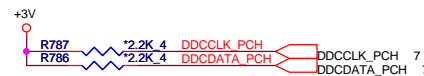
BKLTCTL_PWM

To LVDS Conn.

BKLTEN / LVDDEN

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

SELx	Ay
LOW	B1
HIGH	B2



3/30 Del Location R758 : Pull-done LVDS_BLON_PCH
 3/30 Del Location R759 : Pull-done DISP_ON_PCH
 3/30 Del Location R791 : Pull-done GPU_LVDS_BLON
 3/30 Del Location R790 : Pull-done GPU_DISP_ON

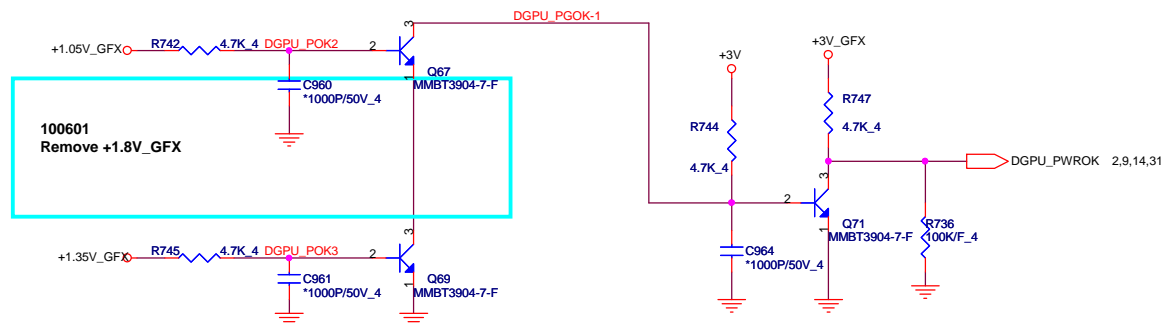
3/30 Del Location U59 : LVDS/CRT DDC Switch

3/30 Del Location U62 : VGA SWITCH

3/30 Del Location U65

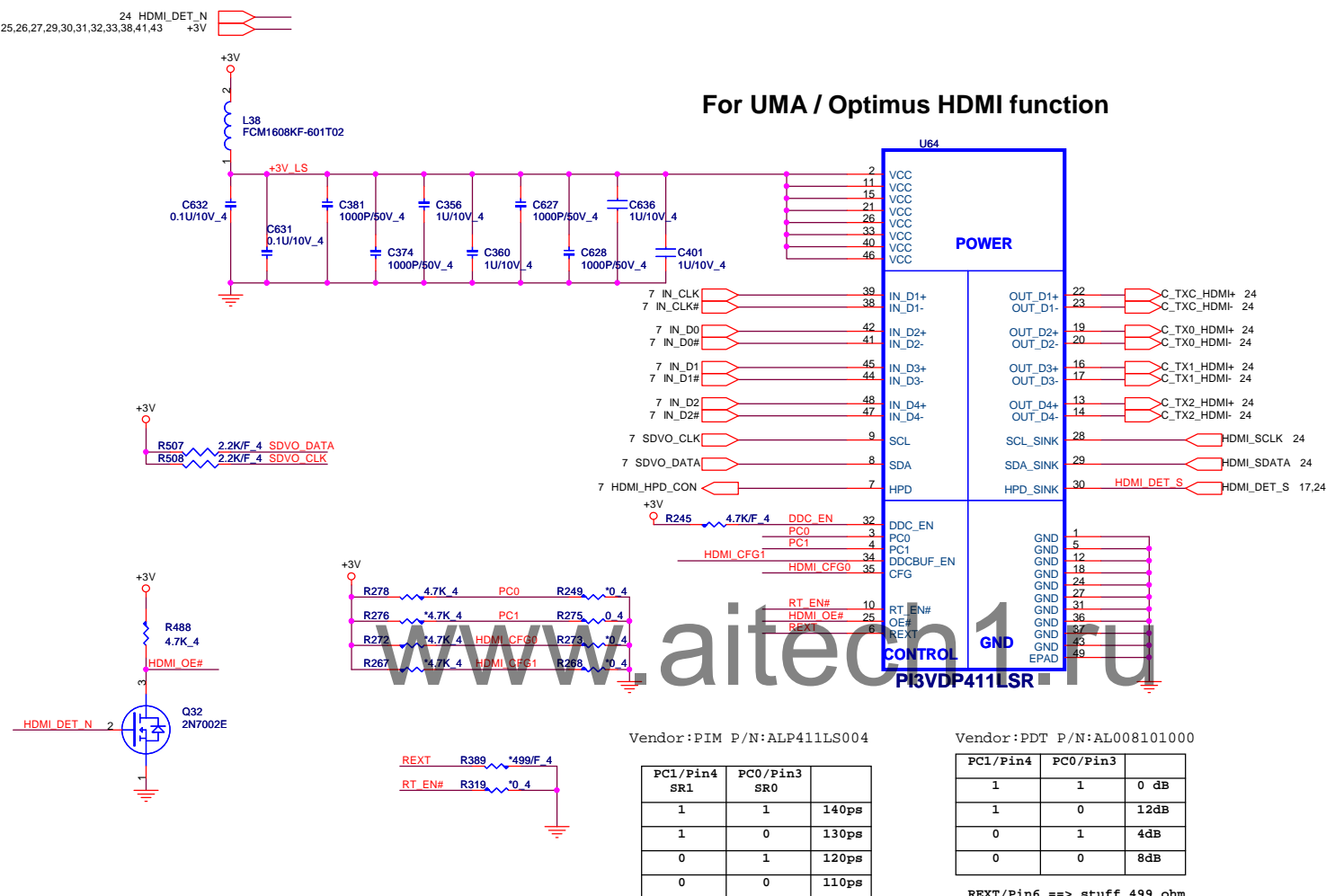
S	Yn
0	B0
1	B1

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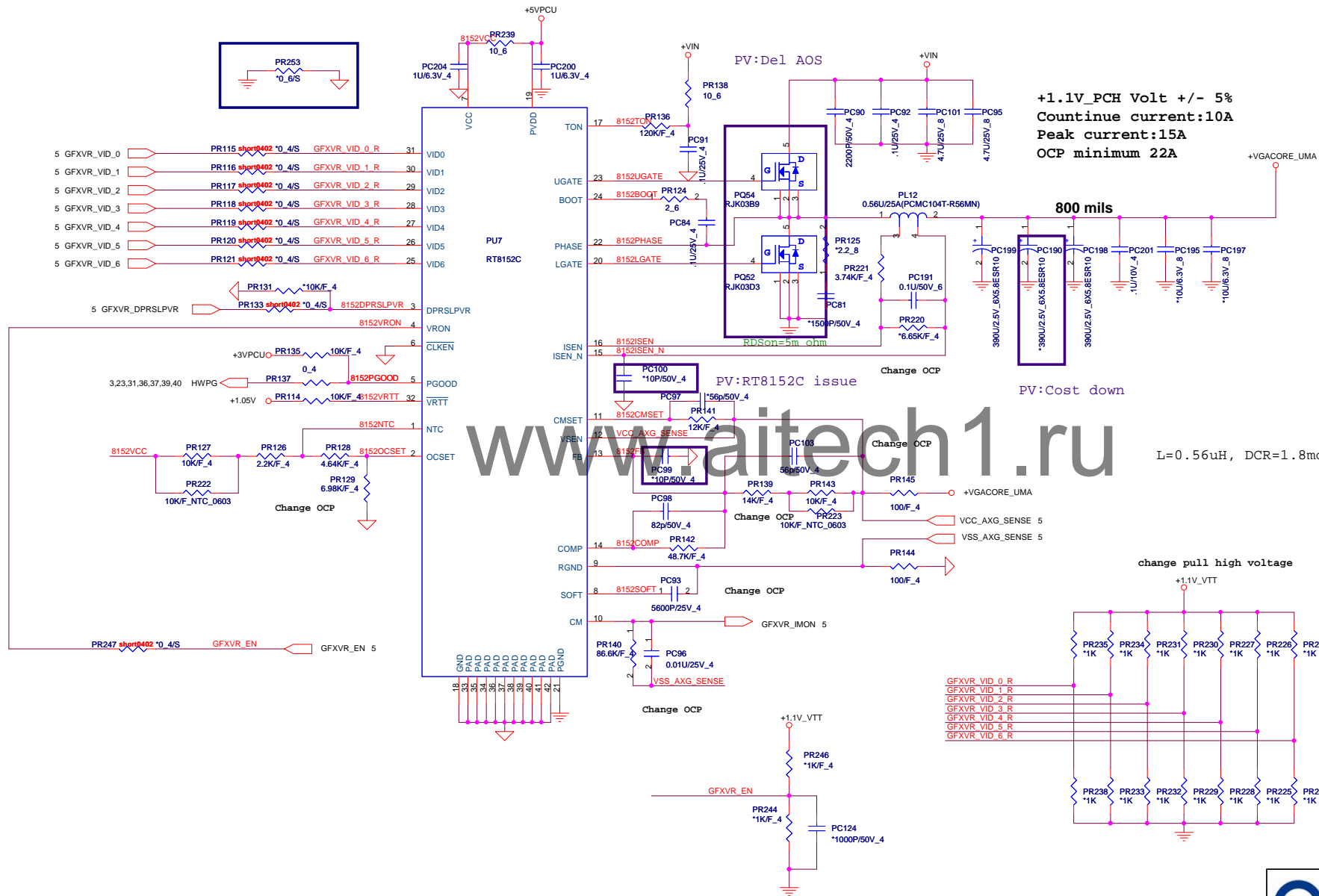
PROJECT : TW9E
 Quanta Computer Inc.

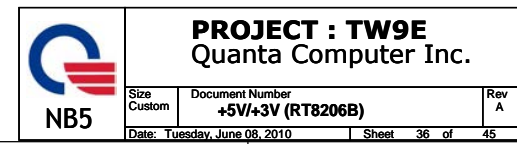
For UMA / Optimus HDMI function

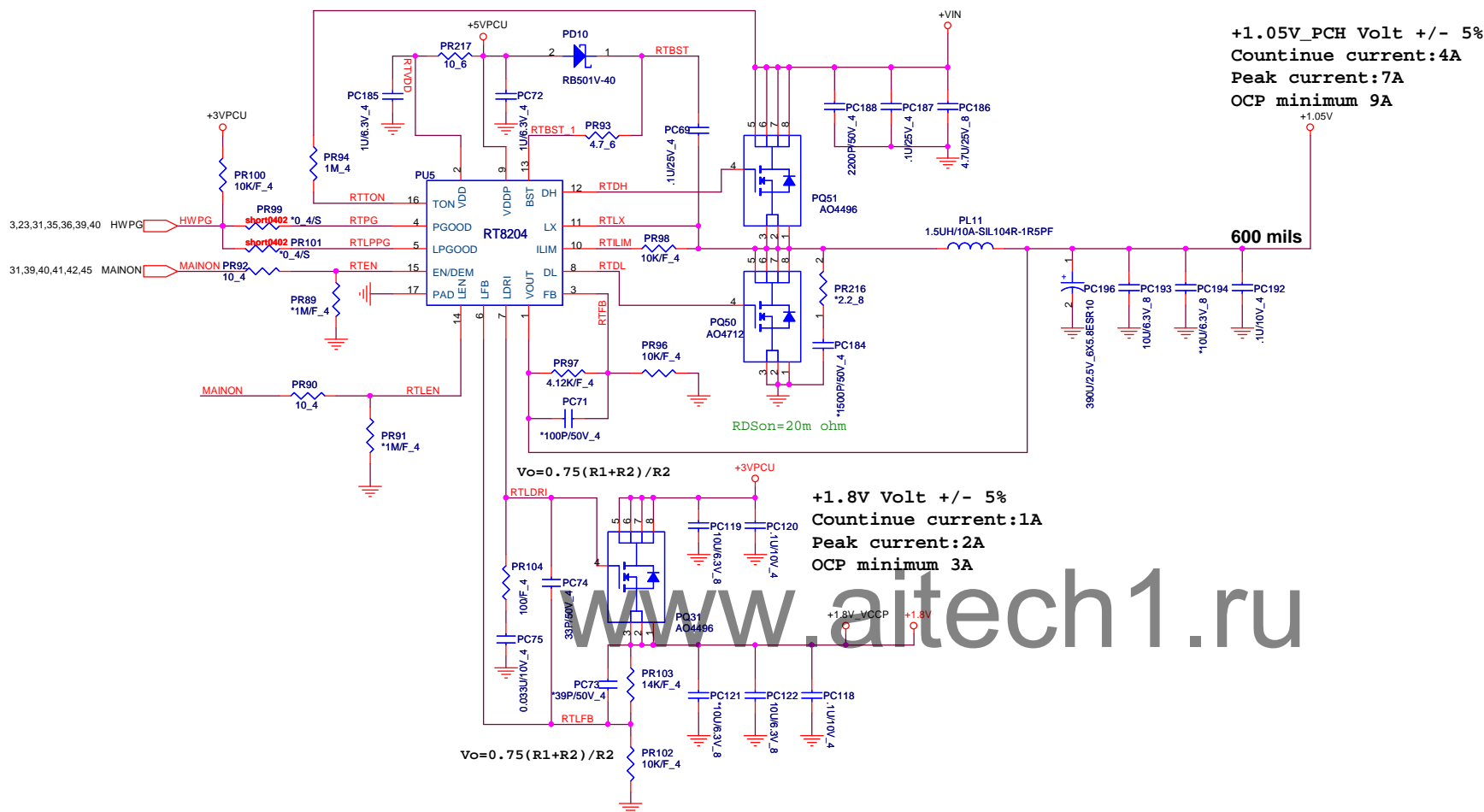


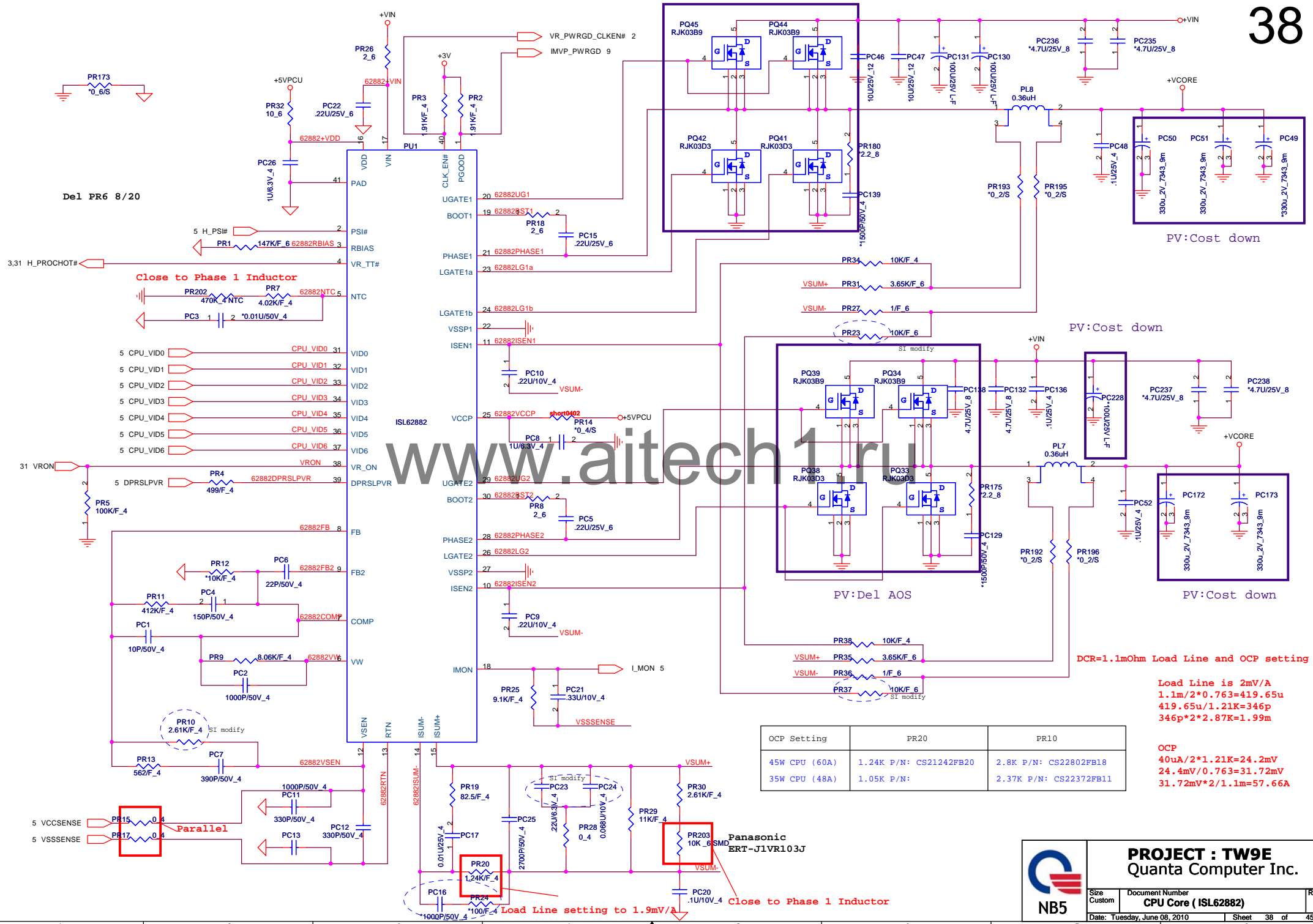
PROJECT : TW9E
Quanta Computer Inc.

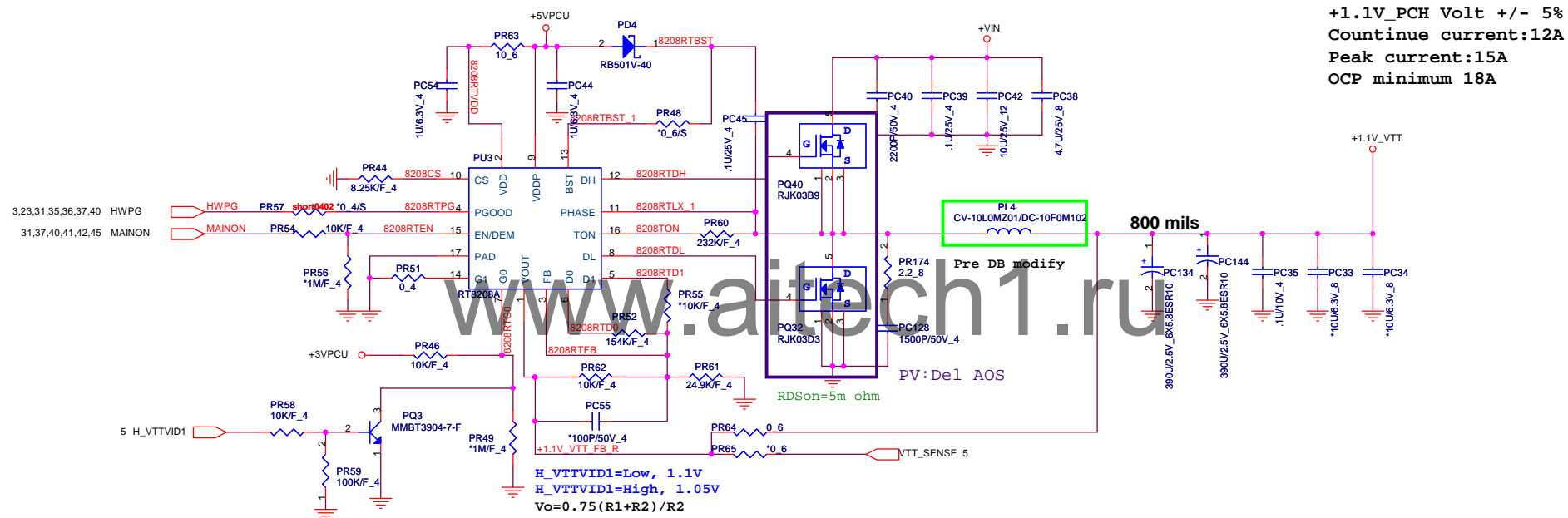
Size	Document Number	Rev
A3	HDMI Switch / Power CRTL	A
Date: Tuesday, June 08, 2010		Sheet 34 of 45





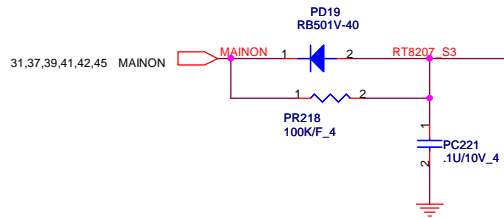
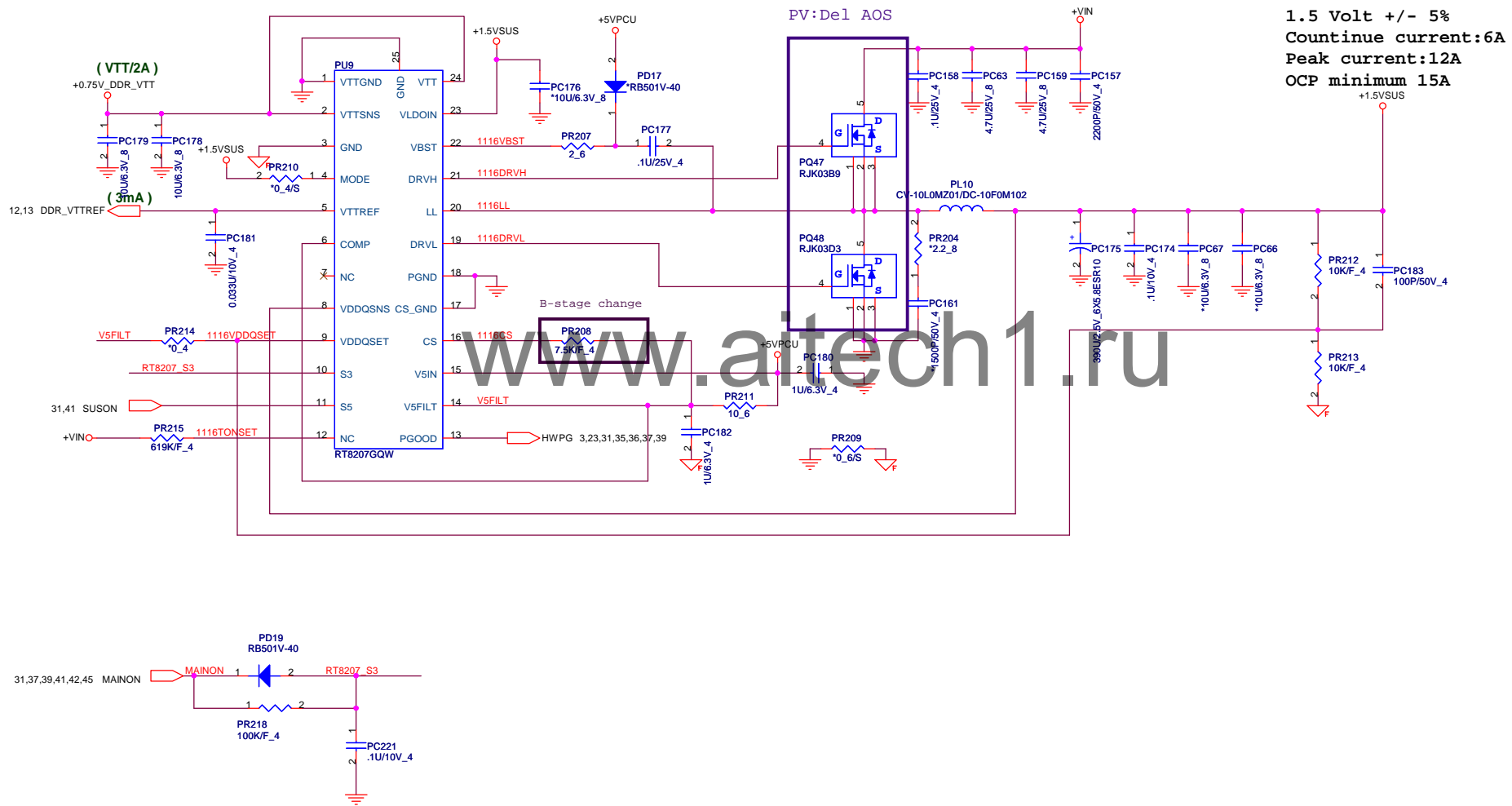


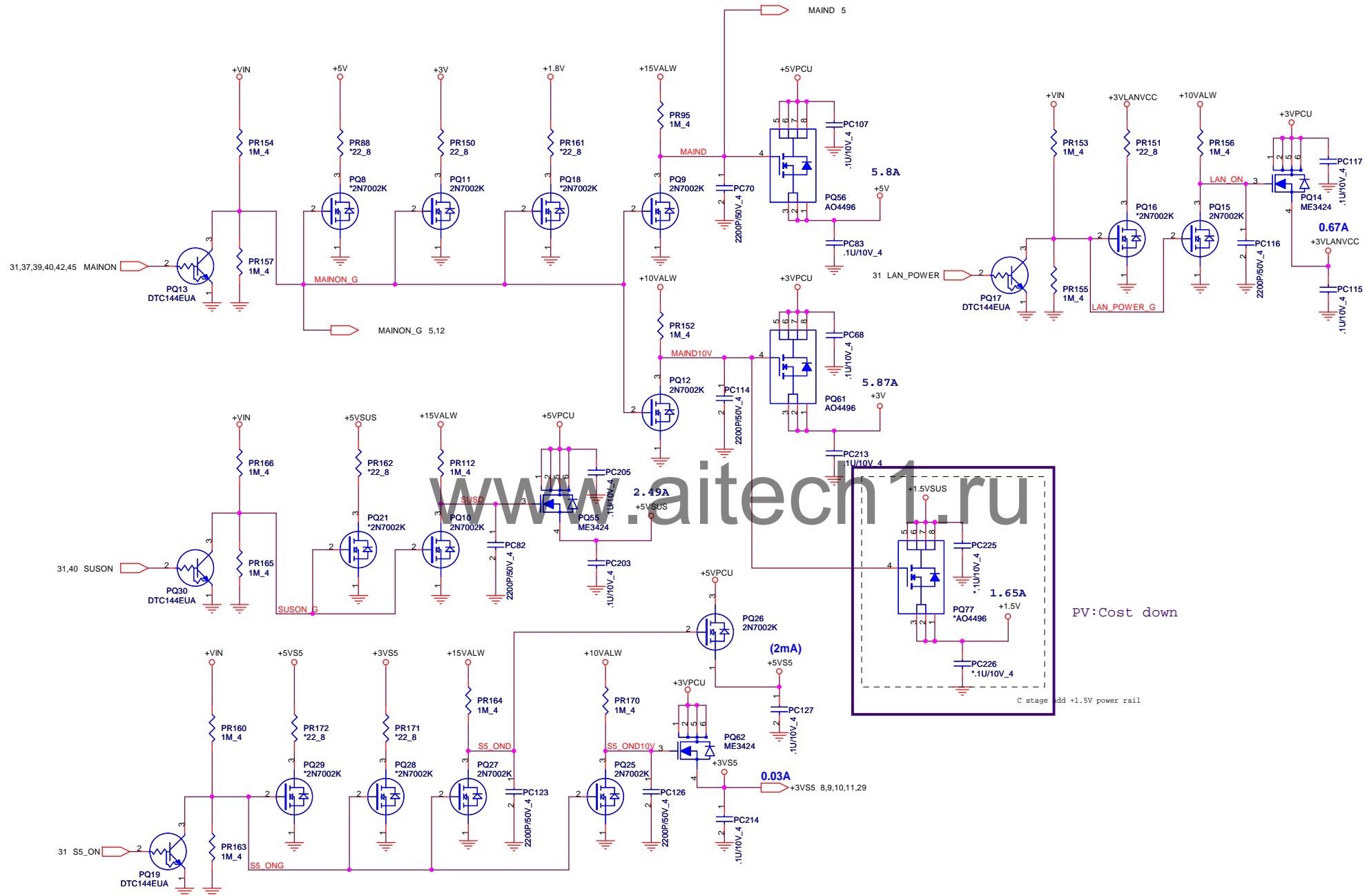


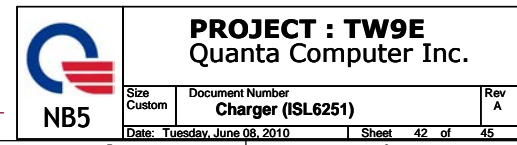


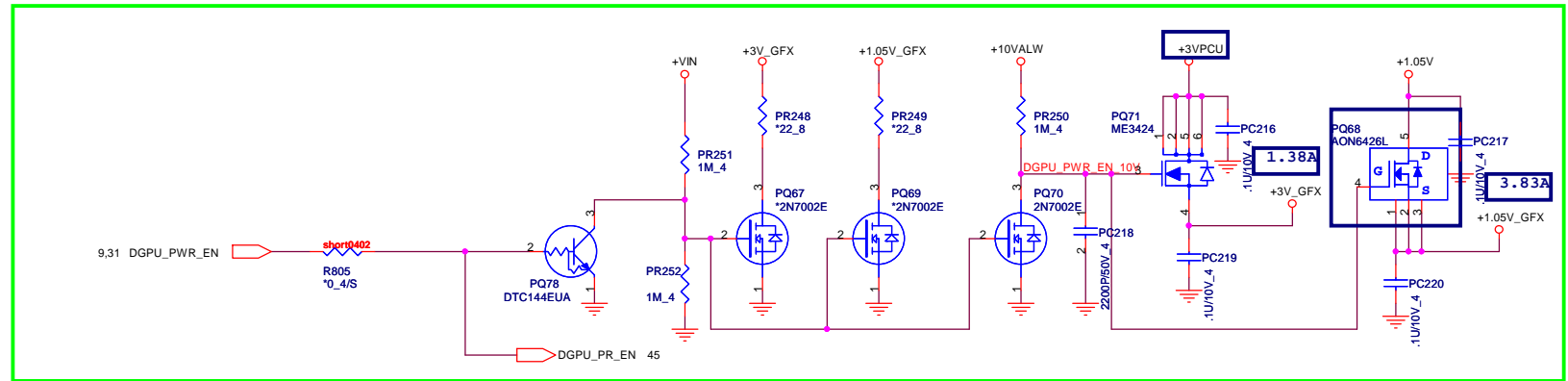
PROJECT : TW9E
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V_VTT/GA Core RT820A	A
Date: Tuesday, June 08, 2010	Sheet 39 of 45	



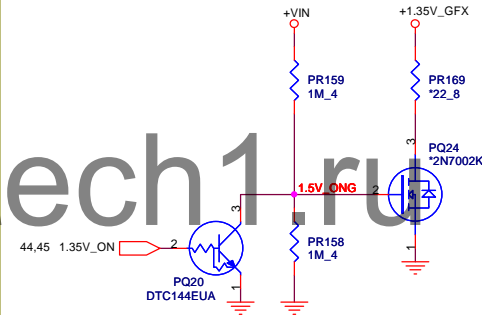






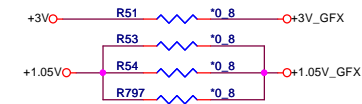
PV:disable +1.8V_VGA

For Discrete or switchable Only



Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete Only



R51 co-lay PQ71
R53/R54 co-lay PQ68

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

For Hybrid DGPU Power Rails Sequence

1. +3V_GFX, +1.05V_GFX
2. +VGA_CORE -> DGPU_PG
3. 1.5V_GFX, +1.8V_GFX



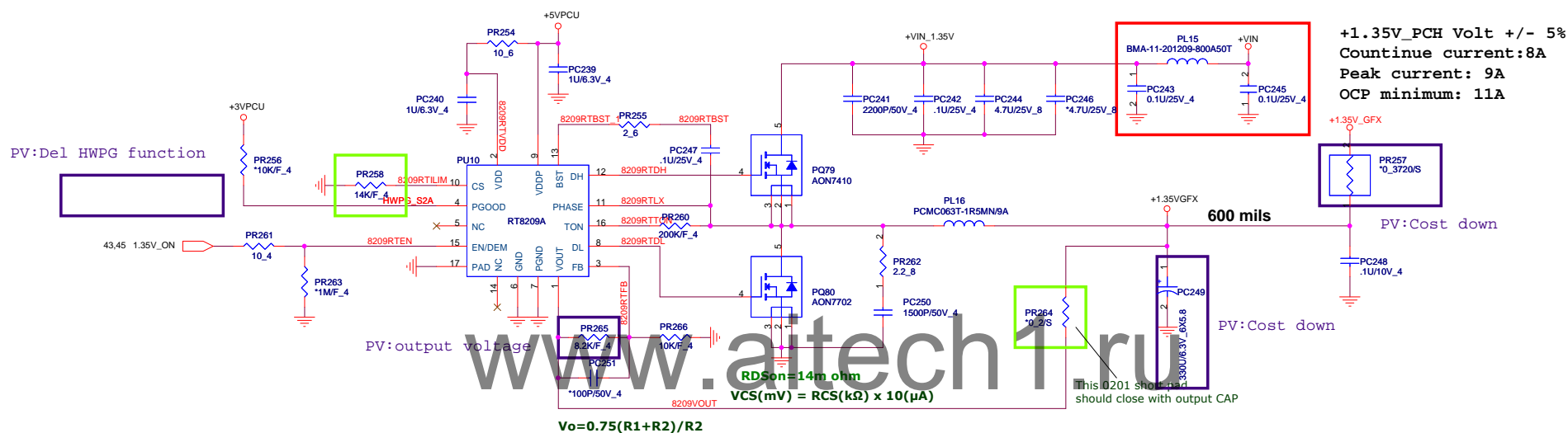
PROJECT : TW9E
Quanta Computer Inc.

Size
A3

Document Number
Switchable Power

Rev
A

Date: Tuesday, June 08, 2010 Sheet 43 of 45



$$V_{out} = (1 + 8.06K/10K) * 0.75 = 1.384V$$

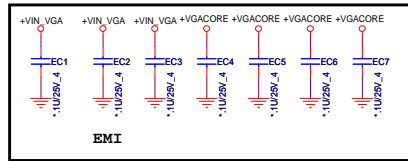
$$OCP = \text{current limit} + I_{out} \text{ ripple} / 2$$

$$= (14K * 10\mu A / 14m \text{ Ohm}) + (2.34/2) = 11A$$

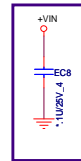
$$R_{ton} = 200K \text{ Ohm} \quad F = 350K \text{ Hz}$$

Nvideo N11E-GE

CNTRL1	CNTRL0	N11E-GE
GPIO6	GPIO5	
0	0	0.9V
0	1	0.85V
1	0	0.8125V
1	1	Don't care

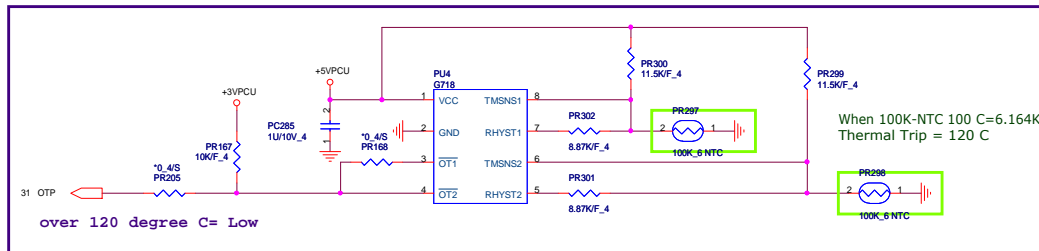
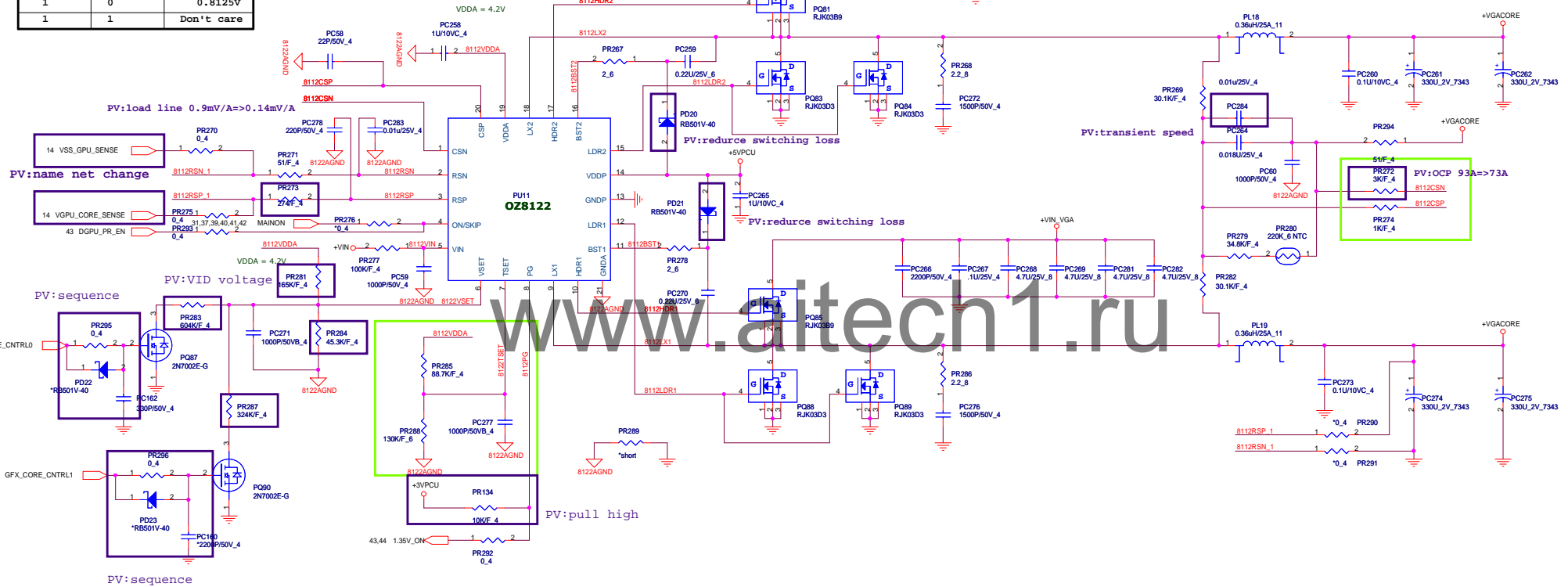
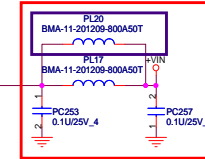


PV:EMI



+VGA_CORE +/- 5%
 Countinue current:43.55A
 Peak current:65.3A
 OCP minimum 70A

PV:power rating



PV:thermal protection